AM08XX/AM18XX Hardware Design Guidelines

1. Introduction

This document describes board level hardware design guidelines for the AM08XX and AM18XX RTC product families. These guidelines should be followed when designing a printed circuit board (PCB) to ensure correct circuit operation and best practices for noise immunity and ESD performance.

2. Schematic and Component Guidelines

This section contains guidelines that should be followed when designing schematics and selecting PCB components.

2.1 Crystal Oscillator

The AMX8XX RTC supports standard 32.768 kHz tuning fork crystals. The 32.768 kHz crystal is directly connected between the XO and XI pins. No external PCB load capacitors are required to tune the crystal frequency because the AMX8XX uses digital calibration to calibrate its internal clocks, which corrects any deviation errors that occur in the 32.768 kHz crystal oscillator circuit frequency. Even though no external load capacitors should be added to the PCB, there will still be a small amount of capacitive loading. The total crystal load capacitance will come from the following sources.

1. AMX8XX XO/XI pin capacitance on each leg of the crystal. This will typically be about 1 pF on each leg.
2. PCB trace capacitance. This occurs due to the PCB trace routing between the crystal and AMX8XX landing pads and the dielectric separating the ground plane underneath. This will typically be in the range of 0.5 – 2.0 pF, dependent upon the PCB layout.
3. Capacitance from the crystal and AMX8XX landing pads. The AMX8XX pin landing pads will be much smaller in area than the trace routing and crystal landing pads and so can be ignored in most cases. The capacitance on each leg of the crystal due to its landing pads will typically be in the range of 0.5 – 3.0 pF.
4. Mutual capacitance between the XO and XI traces that are routed between the AMX8XX and crystal. This is typically 1 pF or less.

Figure 1 below shows the equivalent circuit schematic of the crystal and associated load capacitance attached to the AMX8XX RTC XO and XI pins.

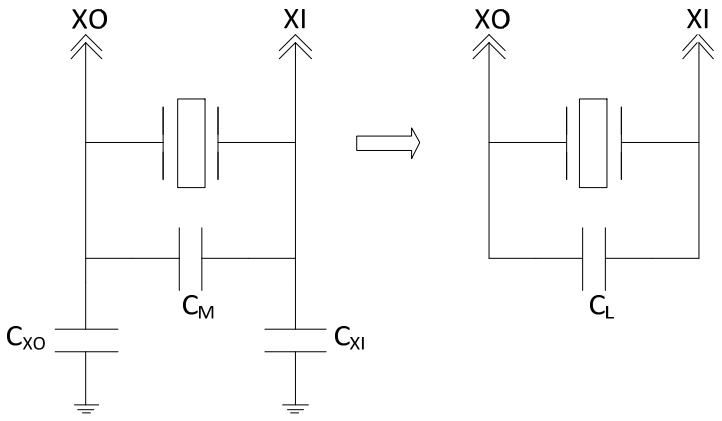


Figure 1 – Crystal Circuit Schematic

Where:

C_M = mutual capacitance between the XO and XI traces

C_{XO} = total capacitance on the XO pin leg of the crystal (the sum of the AMX8XX internal XO pin capacitance, trace capacitance, and crystal landing pad capacitance)

C_{XI} = total capacitance on the XI pin leg of the crystal (the sum of the AMX8XX internal XI pin capacitance, trace capacitance, and crystal landing pad capacitance)

C_L = total external load capacitance seen by the crystal (series combination of C_{XO} and C_{XI}, plus C_M)

$$C_L = \frac{C_{XO} * C_{XI}}{C_{XO} + C_{XI}} + C_M \qquad \textbf{Equation 2-1}$$

The equivalent circuit schematic showing the 4-parameter circuit model for a typical tuning fork crystal including the total external load capacitance, C_L, is shown in Figure 2.

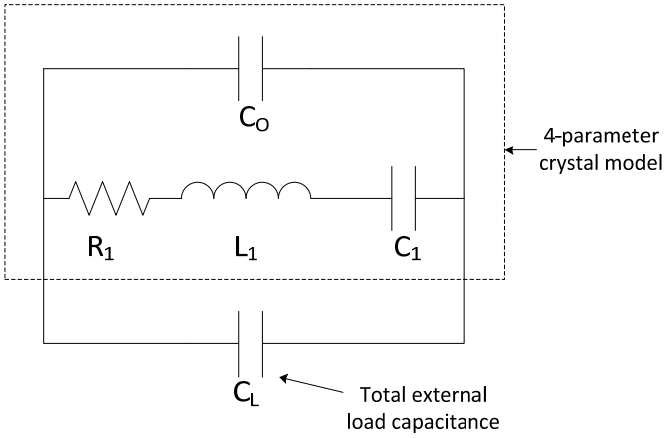


Figure 2 – Crystal Circuit Schematic

Where:

C_O = shunt capacitance of crystal

R_1 = ESR of crystal

L_1 = motion inductance of crystal

C_1 = motion capacitance of crystal

C_L = total external load capacitance given by Equation 2-1

The motion arm of the crystal is the series combination of C_1, L_1, and R_1. The static arm of the crystal is C_O. The motion arm and static arm component values can typically be found in the crystal datasheet.

The series resonant frequency of the crystal, F_s, occurs when the reactance/impedance of the motion arm equals 0 and is given by:

$$F_S = \frac{1}{2\pi\sqrt{L_1 C_1}} \qquad \textbf{Equation 2-2}$$

The crystal circuit frequency, F_L, at a specific parallel load capacitance, C_L, can be derived and is given by:

$$F_L = F_S\sqrt{1 + \frac{C_1}{C_O + C_L}}\ ,\ (R_1 = 0) \qquad \textbf{Equation 2-3}$$

AM08XX/AM18XX Hardware Design Guidelines

Although Equation 2-3 ignores the crystal ESR (R_1), it sufficient for most applications and a more exact expression would complicate calculation of the result without any additional benefit.

Assuming an ideal crystal, F_L will be exactly 32768 Hz when the load capacitance, C_L, matches the recommended loading capacitance specified in the crystal datasheet. Table 1 shows crystals from various manufacturers with recommended load capacitances of 12.5 pF, 9 pF, 7 pF, and 4 pF in a variety of common shapes and sizes.

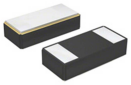
Recommended Load Capacitance (C_L)	12.5 pF	9 pF	7 pF	4 pF
Part #	MS3V-T1R	FC-12D	ST3215SB	ABS06
Manufacturer	Microcrystal	Epson	Kyocera	Abracon
Shunt Capacitance (C_O)	0.9 pF	0.8 pF	0.9 pF	1.47 pF
Motion Capacitance (C_1)	2.1 fF	3.7 fF	3.7 fF	3.869 fF
Size	6.7 x 1.4 mm	2.0 x 1.25 mm	3.2 x 1.5 mm	2.0 x 1.2 mm
Image				

Table 1 – Various Crystals

Using Equation 2-3, the series resonant frequency, F_S, can be calculated using 32768 Hz (0 ppm error) for the crystal circuit frequency, F_L, and the C_1, C_O, and C_L values from the crystal datasheet. For example, the typical series resonant frequency of the Microcrystal MS3V-T1R can be calculated as follows.

$$F_S = \frac{F_L}{\sqrt{1+\frac{C_1}{C_O+C_L}}} = \frac{32768\ Hz}{\sqrt{1+\frac{2.1\ fF}{0.9\ pF+12.5\ pF}}} = 32765.43\ Hz$$

After the series resonant frequency is calculated above, the crystal circuit frequency deviation in terms of ppm relative to 32768 Hz can be plotted vs. load capacitance, C_L, using the following equation:

$$\Delta F_L(\text{ppm}) = \frac{F_S\sqrt{1+\frac{C_1}{C_O+C_L}} - 32768}{32768} * 1000000 \qquad \textbf{Equation 2-4}$$

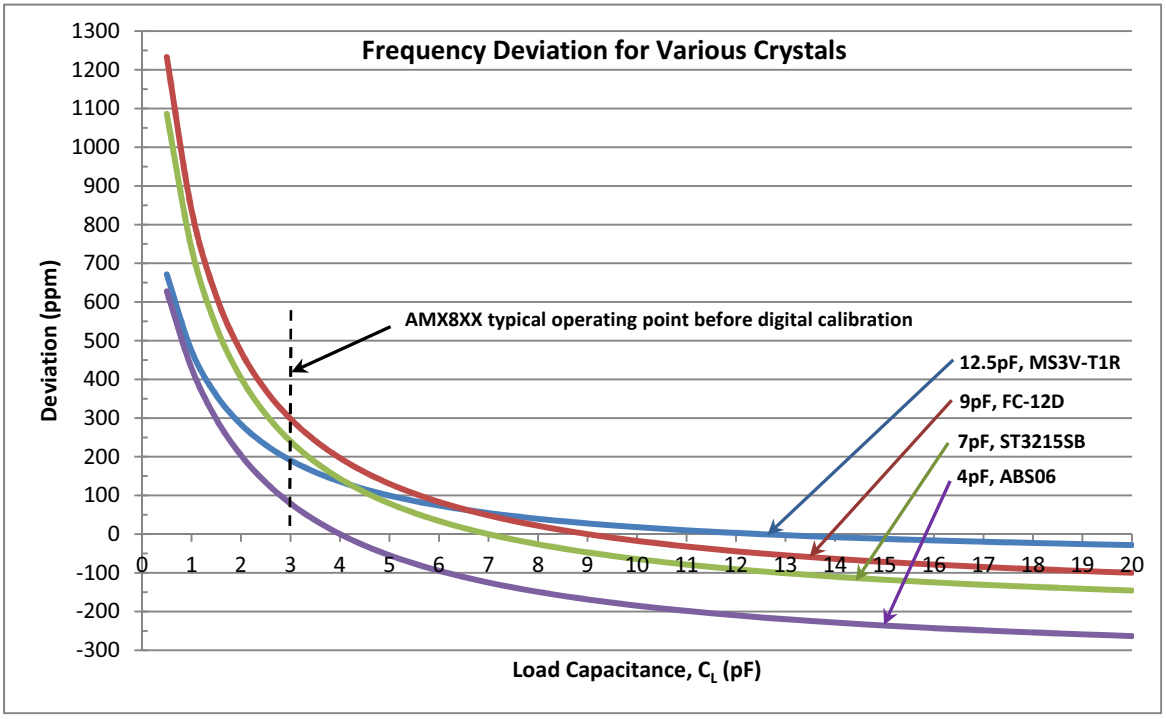
Figure 3 plots the frequency deviation vs. load capacitance using Equation 2-4 for each crystal in Table 1. The curves illustrate that as the load capacitance decreases, the frequency deviation will increase exponentially. In a traditional crystal oscillator circuit, additional capacitors are added to the PCB on each leg of the crystal such that the total equivalent load capacitance matches the recommended load capacitance in the crystal datasheet (for an ideal 0 ppm deviation). Because no external load capacitance is added to the PCB in AMX8XX designs, the resulting load capacitance will typically be much less than the nominal load capacitance specified in the crystal datasheet, which will result in a higher frequency operating point for the AMX8XX. The typical capacitive loading values below with equal loading on each leg of the crystal will produce a total load capacitance of 3 pF. The AMX8XX operating point (before digital calibration) with a crystal load capacitance of 3 pF is shown in Figure 3.

$$C_{XO} = C_{XI} = 1\ pF\ (AMX8XX\ pin) + 1\ pF\ (PCB\ trace) + 2\ pF\ (crystal\ PCB\ landing\ pad) = 4\ pF$$

$$C_M = 1\ pF$$

$$C_L = \frac{C_{XO} * C_{XI}}{C_{XO} + C_{XI}} + C_M = 3\ pF$$

Figure 3 – Crystal Frequency Deviation vs. Load Capacitance



Even though the crystal oscillator circuit operates at a higher frequency due to the lower crystal load capacitance, the AMX8XX XT digital calibration feature allows the internal clocks to be calibrated to within +/- 2 ppm. The XT digital calibration feature has several benefits.

1. Eliminates the need to trim the crystal oscillator frequency by adjusting the load capacitance, which is done in traditional analog solutions.
2. Any crystal oscillator can be used in the circuit without needing to adjust the load capacitance to tune the crystal frequency. The AMX8XX can be digitally calibrated during manufacturing, eliminating any effects of frequency shift due to the variation in the load capacitance and crystal impedance.
3. Reducing the external load capacitance has the added benefit of increasing the oscillation allowance of the crystal oscillator circuit, which aids crystal startup and continued oscillation even as the crystal ESR increases with temperature.

2.2 Autocalibration Filter Capacitor

A 47pF ceramic capacitor should be connected between the AF pin and GND. The capacitor is necessary to filter the AMX8XX analog supply output when operating in RC Autocalibration mode. A standard 47pF ceramic capacitor with a voltage rating of 3.0 V or higher and a tolerance of +/- 20% or less is acceptable.

2.3 Input and Output Pin Resistors

The AMX8XX contains no internal pull-up or pull-down resistors on its input or output pins. Because of this, all unused input pins must be terminated with either a pull-up or pull-down resistor. To reduce external component count, they can also be connected directly to either VCC or GND. Proper termination prevents the voltage on the input pin from floating to mid-level, which can result in higher current on the VCC pin. To prevent addition current draw from VCC, the pull-up or pull-down resistor value should be small enough to overcome any leakage currents required to pull the voltage on the input pin to within at least 400mV of either VCC or GND. In addition, the voltage level must meet the $V_{IH,MIN}$ and $V_{IL,MAX}$ logic requirements of both the host processor and the AMX8XX

RTC. The total leakage current on the input pin will be the sum of I_1 (AMX8XX input pin leakage) and I_2 (pin leakage of the external peripheral device - MCU / host processor, sensor, switch, etc.) as shown in Figure 1. Resistor values between 10 kΩ and 100 kΩ for R_{PU} and R_{PD} are usually acceptable to overcome both sources of leakage current.

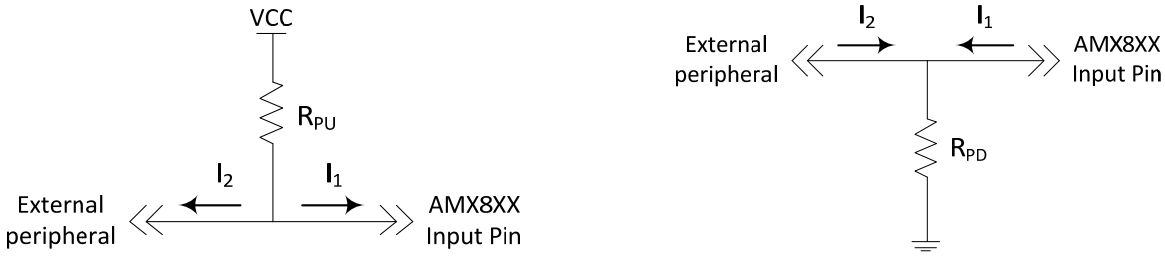


Figure 4 – Pull-up and Pull-down Resistors

Figure 5 shows the typical AMX8XX VCC current change as a function of the input pin voltage both rising above GND and falling below VCC = 3.0V.

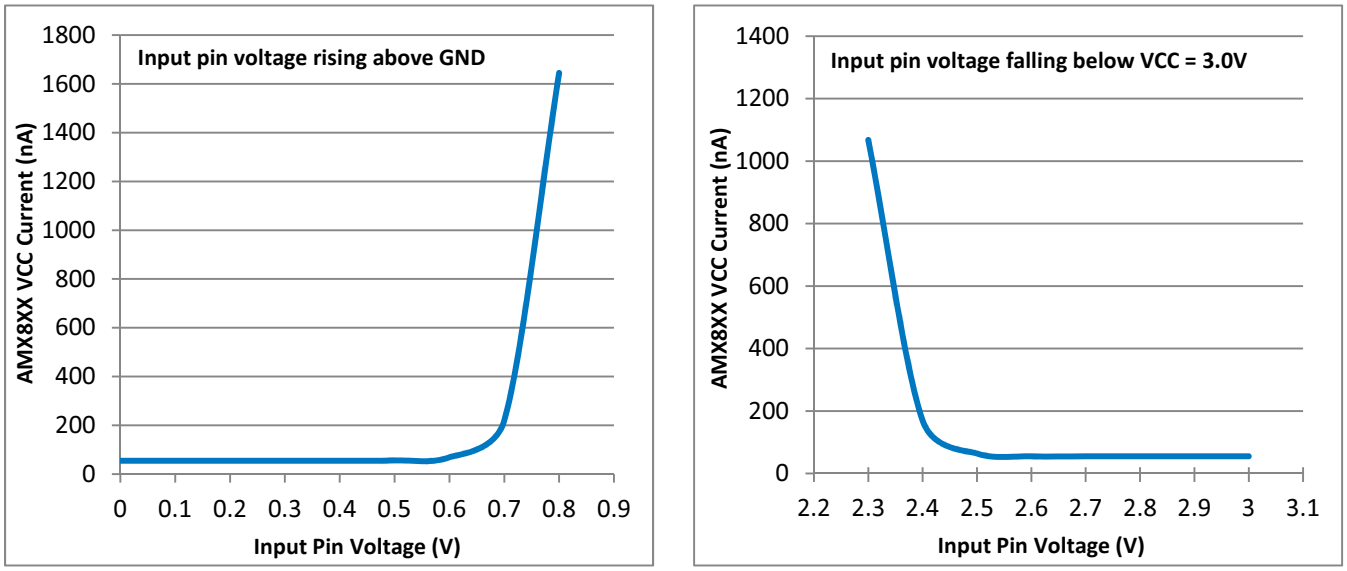


Figure 5 – VCC Current and Input Pin Voltage

As can be seen in Figure 5, the AMX8XX VCC current will increase rapidly when the input pin voltage is greater than 500mV away from either VCC or GND.

The nRST, PSW/nIRQ2, and FOUT/nIRQ output pins are open drain and therefore require an external pull-up resistor to properly create a logic high output. The pull-up resistor value needs to be small enough to overcome the input pin leakage current of the host processor so that the voltage on the pin exceeds the minimum input logic high voltage requirement (to guarantee a valid logic high) when the AMX8XX output pin is high impedance.

2.4 VCC Supply Bypass Capacitors

A capacitor should be used to bypass the AMX8XX VCC supply. The capacitor provides a local source near to the VCC pin to provide instantaneous current to the AMX8XX during switching conditions. This is particularly important when an output pin switches high (to the VCC rail) and must drive pin and PCB trace capacitance. Because the AMX8XX current consumption is extremely low and has a small number of output pins that all

operate at relatively low frequencies, a small ceramic capacitor, 0.1 µF, can be used to bypass the VCC supply. If additional VCC capacitance is required due to other system components, care should be taken to keep the total capacitor leakage current as low as possible.

When the AMX8XX RTC is running with currents of only tens of nanoamps, one important factor that can be easily overlooked is the capacitor leakage current or insulation resistance. The leakage current of large value capacitors can exceed the AMX8XX operating current in some cases. An equivalent low frequency circuit model (not including inductive effects) for a ceramic capacitor is shown below in Figure 6.

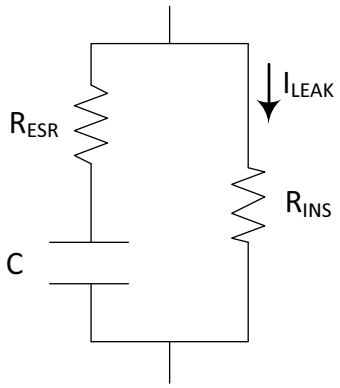


Figure 6 – Low Frequency Capacitor Model

Where:

R_{ESR} = equivalent series resistance (ESR)

R_{INS} = insulation resistance

I_{LEAK} = leakage current due to insulation resistance

C = capacitance value

A ceramic capacitor ESR is typically under 0.1 ohms. In some cases, the capacitor ESR must be taken into consideration when dealing with very high peak currents and the resulting voltage drop across R_{ESR}. However, due to the ultra-low current consumption of the AMX8XX, R_{ESR} can be ignored.

The insulation resistance of a ceramic capacitor represents the ratio between the applied voltage and the leakage current after a set period of time. In ceramic capacitor datasheets, this is usually specified in megohms (MΩ) or ohm-farads (Ω-F) and tested at the rated voltage after 1-2 minutes.

Immediately after a DC voltage is applied to the capacitor, an inrush (charge) current will occur. The absorption current occurs due to the dielectric loss of the capacitor and decreases exponentially with time. The leakage current is then measured as the constant current flowing through the capacitor after the absorption current has decreased to an acceptable level.

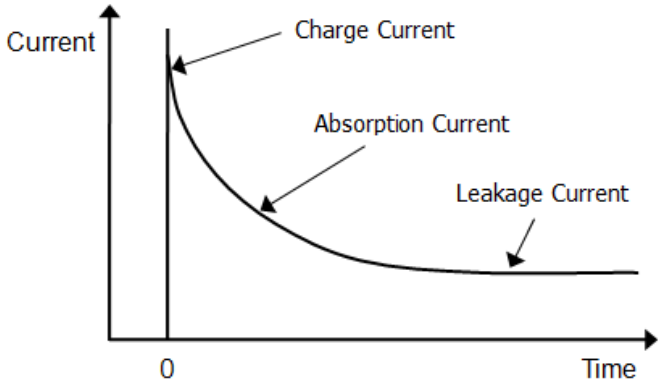


Figure 7 – Ceramic Capacitor Current Profile

As can be seen in the ceramic capacitor current profile curve in Figure 7, to properly specify the insulation resistance or leakage current, the timing of the measurement after the applied voltage (at time = 0) must also be specified.

Ambiq Micro has tested the leakage currents of large value ceramic capacitors ranging from 10-100µF. Table 2 shows typical leakage currents of the capacitors 10 minutes after applying 3.3V across the capacitor terminals at room temperature.

Capacitor Value (µF)	Package Case Code	Size (mm) (LxWxH)	Leakage Current (nA)
100	1206	3.2x1.6x1.6	11
47	0805	2.0x1.25x.95	5.5
22	0603	1.6x0.8x0.8	2.6
10	0402	1.0x0.5x0.7	1.1

Table 2 – Ceramic Capacitor Leakage Currents

The ceramic capacitor leakage currents may be slightly different than those in Table 2 dependent upon the manufacturer and product variation. Notice that the leakage current of a typical 100 µF ceramic capacitor will be approximately equivalent to the AMX8XX operating current in RC oscillator mode. Lower leakage capacitors can also be obtained with tradeoffs between cost and size. The ceramic capacitor manufacturer should be consulted for insulation resistance specifications and system testing performed to determine the system specific leakage current. Because a ceramic capacitor with a value of 0.1 µF can be used to bypass the AMX8XX supply, the leakage current of the bypass capacitor is typically insignificant.

2.5 VBAT Supply ESR

For VBAT switchover applications, a back-up supply (capacitor, supercapacitor, coin-cell battery, etc.) is attached to the VBAT pin of the AMX8XX. When the VCC supply is removed, the AMX8XX will automatically switch over to the back-up supply on the VBAT pin. To ensure correct switchover to the back-up supply under all operating conditions, the total series resistance (ESR) of the back-up supply should nominally be 1.5 kohms (1.0 kohms minimum). Most back-up supplies have an ESR that is much lower than this, which will require an external resistor, R10, in series with the VBAT back-up supply as shown in the reference schematics in section 2.6.

2.6 Reference Schematics

Figure 8 and Figure 9 show reference schematics for the AMX8XX family superset parts, the AM1805 (I^2C) and AM1815 (SPI). Note that some of the pins will be no-connect (NC) dependent upon the AMX8XX product family member used in the design. No-connect pins do not require pull-up resistors and should remain floating.

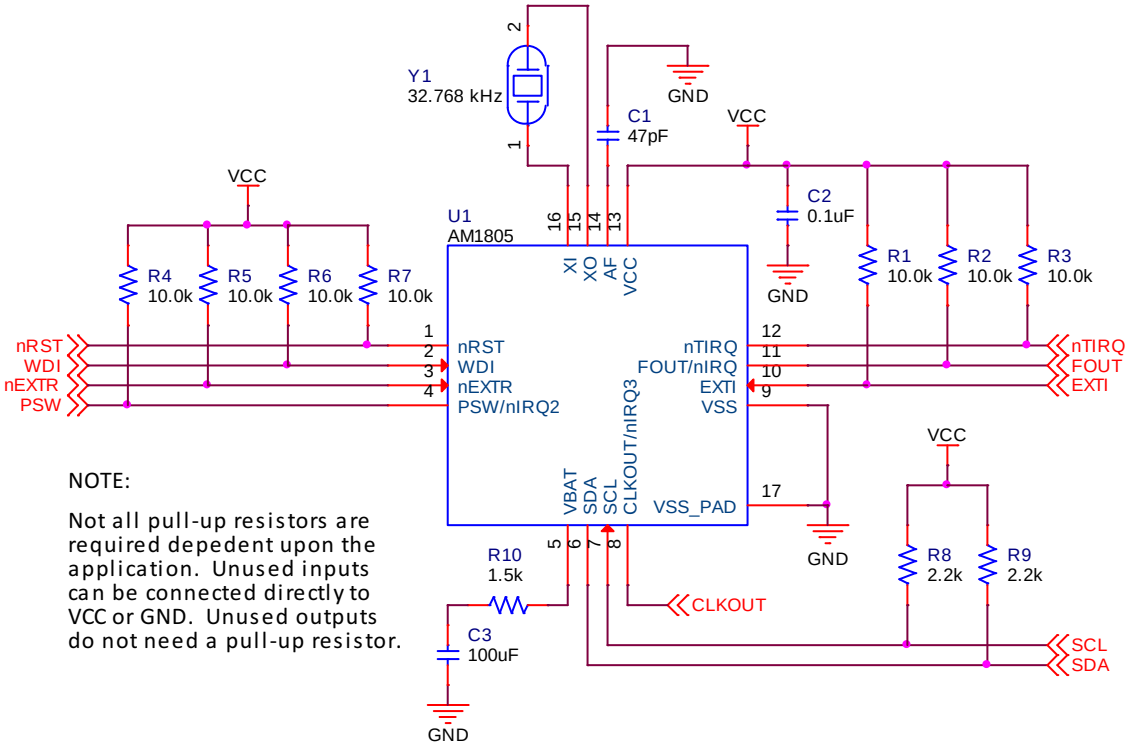


Figure 8 – I²C Reference Schematic

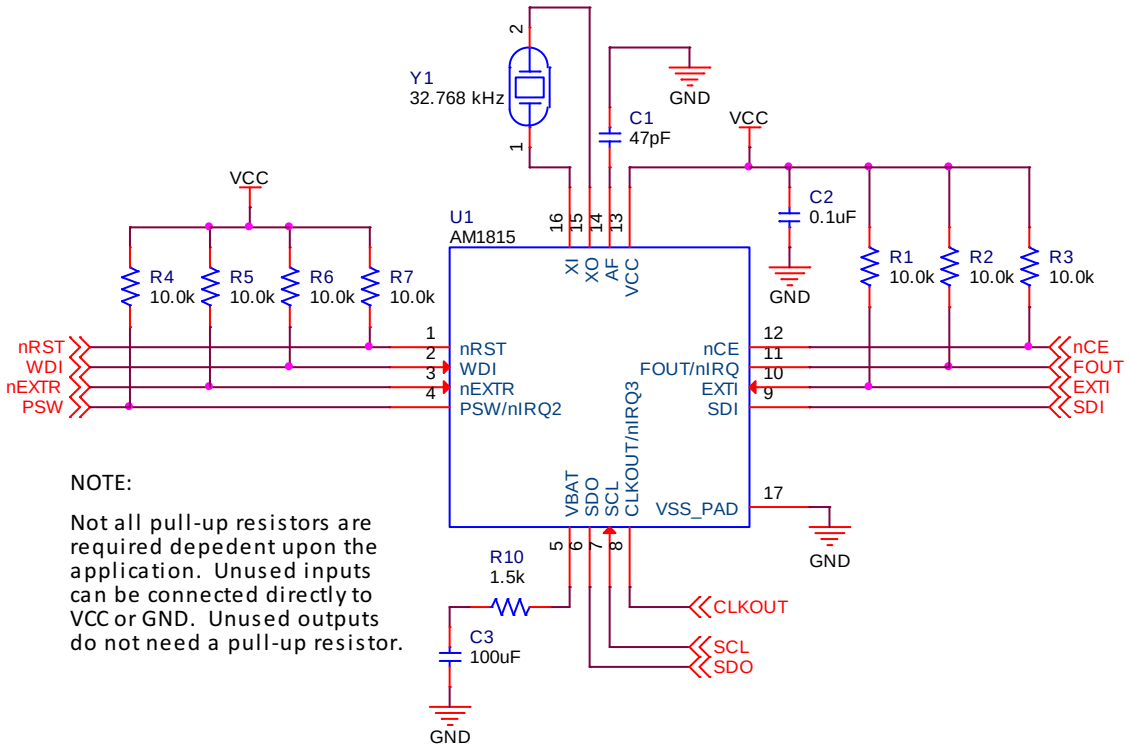


Figure 9 – SPI Reference Schematic

3. Layout Guidelines

This section contains guidelines that should be followed when designing a PCB layout to support the AMX8XX. Topics include component placement, trace routing, ground and power planes, PCB stack-up, and a reference layout.

3.1 Checklist

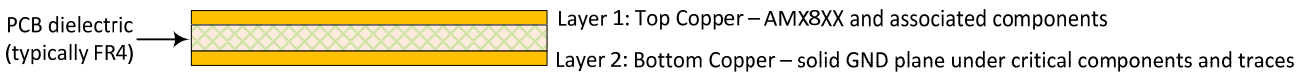
Below is a checklist of important layout guidelines that should be followed when incorporating the AMX8XX into a PCB design.

1. The 32.768 kHz crystal should be placed as close as possible to the XO/XI pins. Although not required, if pads for external load capacitors are placed on the board, they should also be placed as close as possible to the crystal and XO/XI pins to maintain a tight crystal oscillator circuit layout.
2. It is extremely important that a solid ground plane be placed under the entire crystal oscillator circuit. This includes the crystal component and its associated PCB landing pads, the AMX8XX XO and XI pin PCB landing pads, and the entire trace route between the two components. No other traces should be routed underneath the crystal oscillator circuit. A solid ground plane will aid in shielding the crystal oscillator circuit, which will improve the ESD performance, prevent coupling from nearby traces, and make the circuit less susceptible to electromagnetic interference (EMI).
3. The AMX8XX QFN package thermal pad should be connected directly to the sold ground plane. This creates a low impedance GND connection between the AMX8XX and PCB ground plane and also provides additional shielding of the die.
4. A supply bypass capacitor should be placed as close as possible to the AMX8XX VCC pin. Selection of the bypass capacitor and total VCC capacitance should be carefully considered as described in section 2.4. The supply bypass capacitor also helps to stabilize the VCC rail during high current or voltage transients that can occur in an ESD event.
5. The 47pF filter capacitor must be placed as close as possible to the AF pin (16-QFN package pin 14) of the AMX8XX. This capacitor filters the internal analog supply when operating in autocalibration mode. Because the AF pin is a high impedance output, a solid ground plane should be placed underneath this capacitor and associated PCB trace routing to provide shielding and prevent coupling from nearby traces on the board.

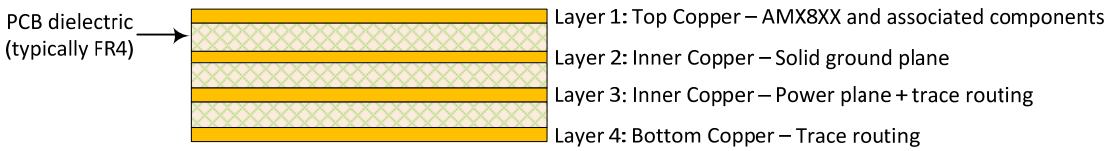
3.2 PCB Layer Stack-up and Planes

To make it easier to implement the crystal circuit and AF filter capacitor ground plane shielding guidelines in section 3.1, the PCB layer stack ups below are recommended. It will also help to improve the EMI and ESD performance of the system. The key aspect of each layer stack-up is that a solid ground plane is placed underneath the AMX8XX RTC.

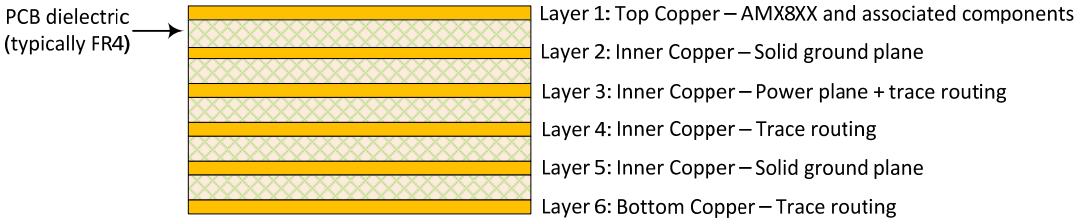
2 Layer PCB Stack-up:



4 Layer PCB Stack-up:



6 Layer PCB Stack-up:



3.3 Reference Layout

The recommended 2 layer PCB layout using the AM1805 I^2C reference schematics from section 2.6 is shown in Figure 10 below. All components are placed on the top layer (show in blue color). On the bottom layer (shown in gray color) a thick VCC trace is used to connect power to the AM1805 VCC pin and the I/O pin pull-up resistors. The key item to follow from the reference layout below is that a solid ground place is placed underneath the entire crystal circuit, AF pin filter capacitor circuit, and the AM1805 RTC. The VCC trace and other PCB routing should avoid these areas.

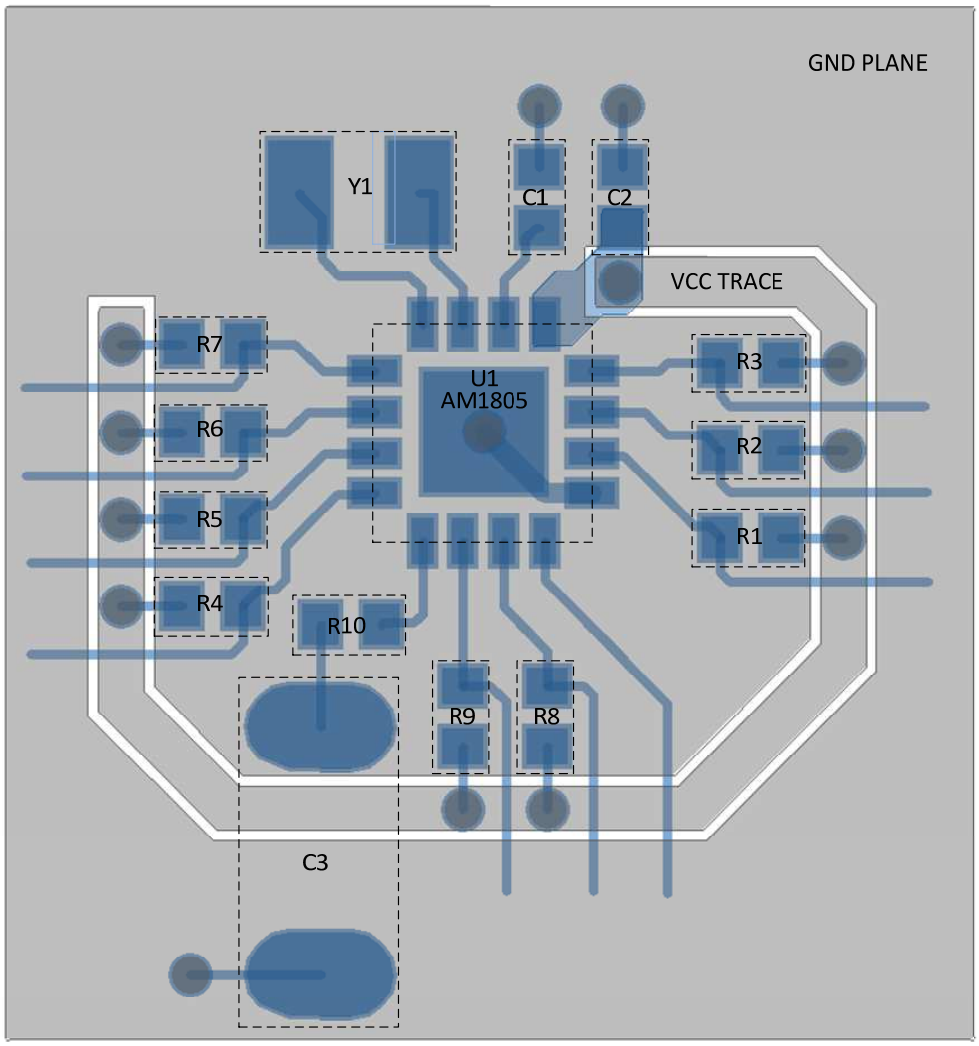


Figure 10 – AM1805 Reference Layout

Document Revision History

Rev #	Description
1.0	Initial release

Contact Information

Address:

Ambiq Micro, Inc.
303 Camp Craft Road
Westlake Hills, TX 78746

+1 (512) 394-8542

Website: www.ambiqmicro.com

General Information: info@ambiqmicro.com

Sales: sales@ambiqmicro.com

Technical Support: support@ambiqmicro.com