# MC10H141

# Four-Bit Universal Shift Register

**ON Semiconductor®**

**http://onsemi.com**

### Description

The MC10H141 is a four−bit universal shift register. This device is a functional/pinout duplication of the standard MECL 10K™ part with 100% improvement in propagation delay and operation frequency and no increase in power supply current.

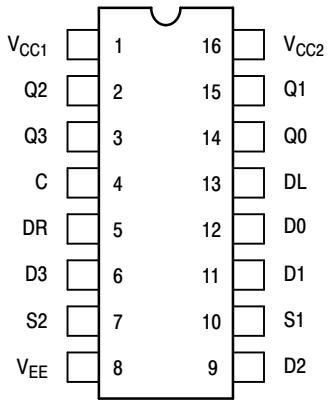
### Features

- Shift frequency, 250 MHz Min
- Power Dissipation, 425 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K Compatible
- Pb−Free Packages are Available*

**Table 1. TRUTH TABLE**

| SELECT | | OPERATING MODE | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| S1 | S2 | | $Q0_{n+1}$ | $Q1_{n+1}$ | $Q2_{n+1}$ | $Q3_{n+1}$ |
| L | L | Parallel Entry | D0 | D1 | D2 | D3 |
| L | H | Shift Right* | $Q1_n$ | $Q2_n$ | $Q3_n$ | DR |
| H | L | Shift Left* | DL | $Q0_n$ | $Q1_n$ | $Q2_n$ |
| H | H | Stop Shift | $Q0_n$ | $Q1_n$ | $Q2_n$ | $32_n$ |

* Outputs as exist after pulse appears at “C” input with input conditions as shown (Pulse Positive transition of clock input).

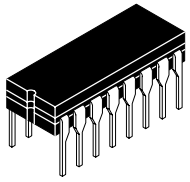


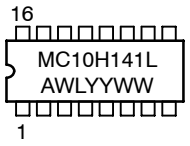

Pin assignment is for Dual−in−Line Package.

**Figure 1. Pin Assignment**

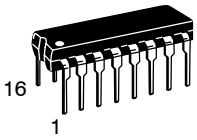
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

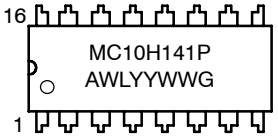
**MARKING DIAGRAMS***



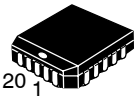


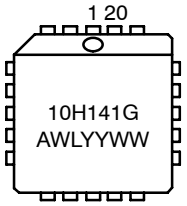

**CDIP−16**
**L SUFFIX**
**CASE 620A**




**PDIP−16**
**P SUFFIX**
**CASE 648**




**PLLC−20**
**FN SUFFIX**
**CASE 775**

| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*For additional marking information, refer to Application Note AND8002/D.

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

**Table 2. MAXIMUM RATINGS**

| Symbol | Characteristic | Rating | Unit |
|---|---|---|---|
| $V_{EE}$ | Power Supply ($V_{CC}$ = 0) | −8.0 to 0 | Vdc |
| $V_I$ | Input Voltage ($V_{CC}$ = 0) | 0 to $V_{EE}$ | Vdc |
| $I_{out}$ | Output Current – Continuous<br>– Surge | 50<br>100 | mA |
| $T_A$ | Operating Temperature Range | 0 to +75 | °C |
| $T_{stg}$ | Storage Temperature Range – Plastic<br>– Ceramic | −55 to +150<br>−55 to +165 | °C<br>°C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

**Table 3. ELECTRICAL CHARACTERISTICS** ($V_{EE}$ = −5.2 V ±5% (Note 1)

| | | 0° | | 25° | | 75° | | |
|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Max | Min | Max | Min | Max | Unit |
| $I_E$ | Power Supply Current | – | 112 | – | 102 | – | 112 | mA |
| $I_{inH}$ | Input Current High<br>Pins 5,6,9,11,12,13<br>Pins 7,10<br>Pin 4 | <br>–<br>–<br>– | <br>405<br>416<br>510 | <br>–<br>–<br>– | <br>255<br>260<br>320 | <br>–<br>–<br>– | <br>255<br>260<br>320 | μA |
| $I_{inL}$ | Input Current Low | 0.5 | – | 0.5 | – | 0.3 | – | μA |
| $V_{OH}$ | High Output Voltage | −1.02 | −0.84 | −0.98 | −0.81 | −0.92 | −0.735 | Vdc |
| $V_{OL}$ | Low Output Voltage | −1.95 | −1.63 | −1.95 | −1.63 | −1.95 | −1.60 | Vdc |
| $V_{IH}$ | High Input Voltage | −1.17 | −0.84 | −1.13 | −0.81 | −1.07 | −0.735 | Vdc |
| $V_{IL}$ | Low Input Voltage | −1.95 | −1.48 | −1.95 | −1.48 | −1.95 | −1.45 | Vdc |

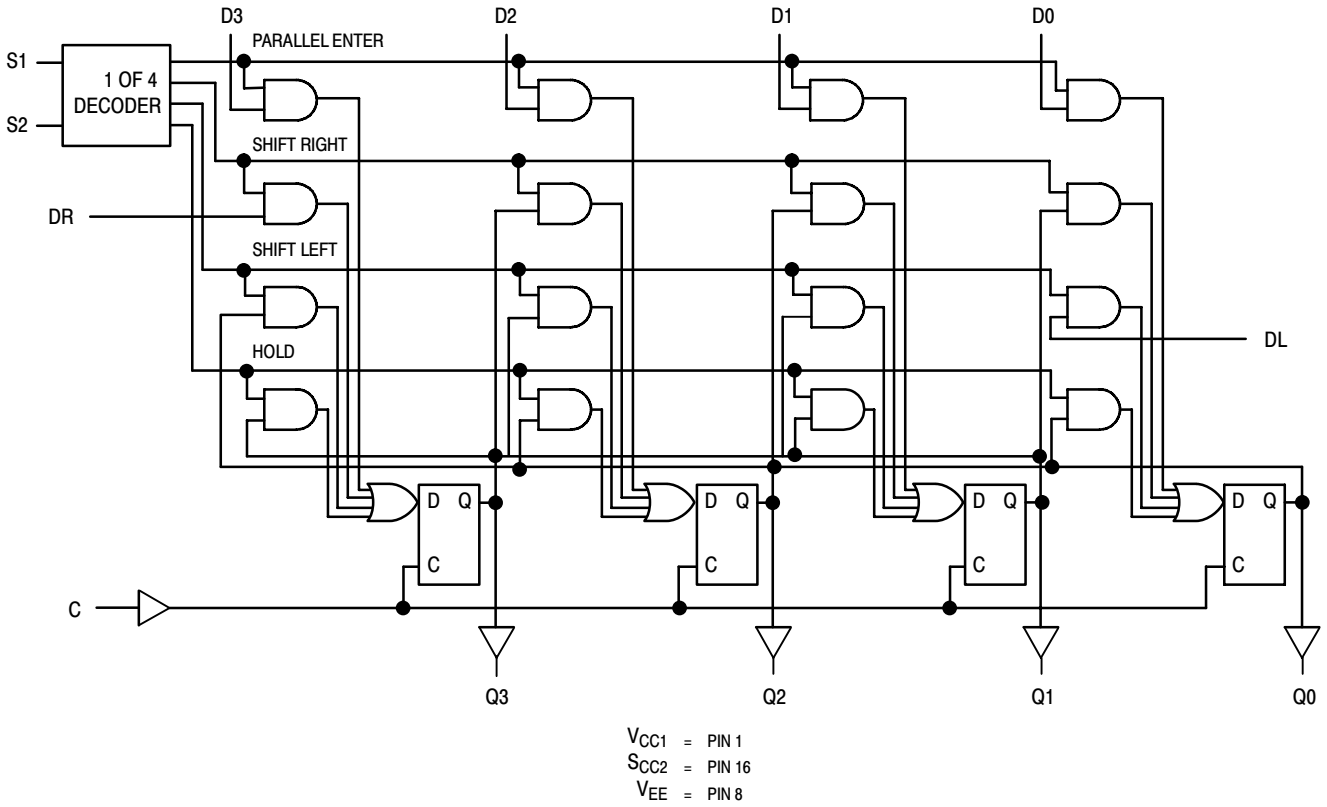
1. Each MECL 10H™ series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.

**Table 4. AC PARAMETERS**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation Delay | 1.0 | 2.0 | 1.0 | 2.0 | 1.1 | 2.1 | ns |
| $t_{hold}$ | Hold Time –<br>Data, Select | 1.0 | – | 1.0 | – | 1.0 | – | ns |
| $t_{set}$ | Set−up Time<br>Data<br>Select | <br>1.5<br>3.0 | <br>–<br>– | <br>1.5<br>3.0 | <br>–<br>– | <br>1.5<br>3.0 | <br>–<br>– | ns |
| $t_r$ | Rise Time | 0.5 | 2.4 | 0.5 | 2.4 | 0.5 | 2.4 | ns |
| $t_f$ | Fall Time | 0.5 | 2.4 | 0.5 | 2.4 | 0.5 | 2.4 | ns |
| $f_{shift}$ | Shift Frequency | 250 | – | 250 | – | 250 | – | MHz |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

## LOGIC DIAGRAM




## APPLICATION INFORMATION

The MC10H141 is a four−bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip−flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

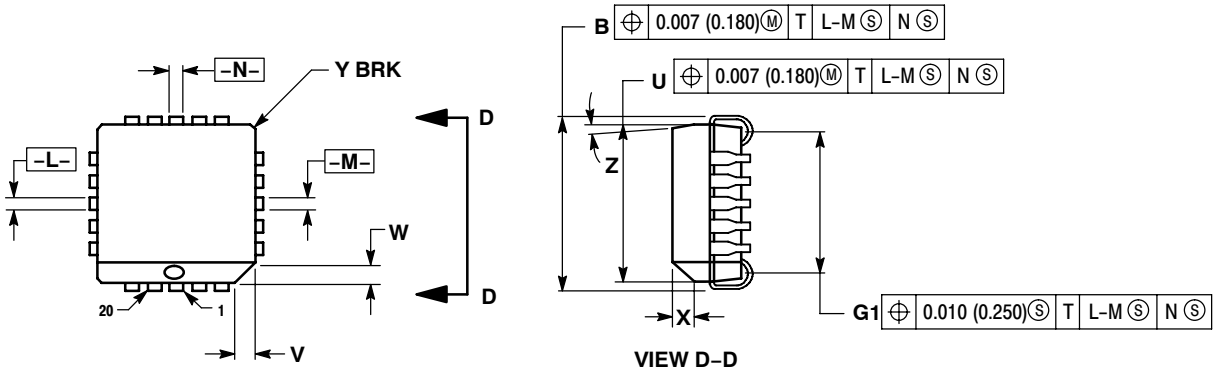
### ORDERING INFORMATION

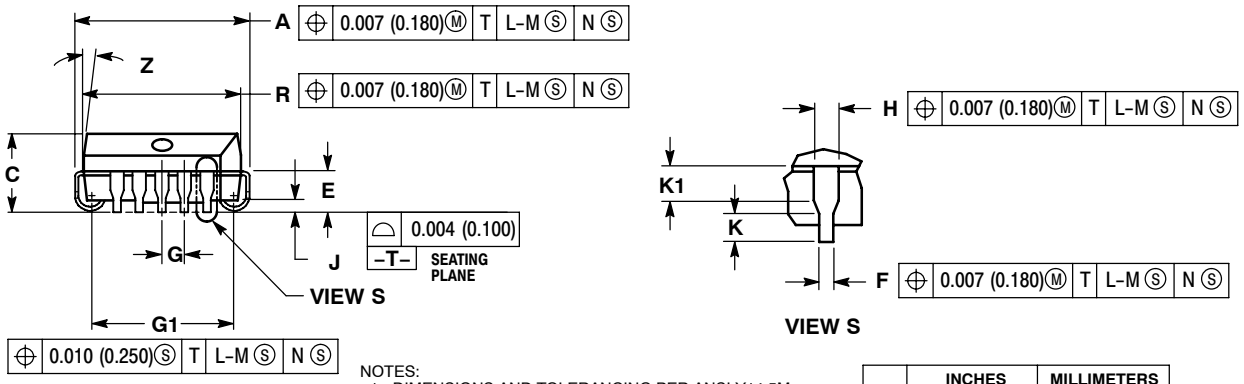
| Device | Package | Shipping† |
|---|---|---|
| MC10H141FN | PLLC−20 | 46 Units / Rail |
| MC10H141FNG | PLLC−20<br>(Pb−Free) | 46 Units / Rail |
| MC10H141FNR2 | PLLC−20 | 500 / Tape & Reel |
| MC10H141FNR2G | PLLC−20<br>(Pb−Free) | 500 / Tape & Reel |
| MC10H141L | CDIP−16 | 25 Unit / Rail |
| MC10H141P | PDIP−16 | 25 Unit / Rail |
| MC10H141PG | PDIP−16<br>(Pb−Free) | 25 Unit / Rail |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**20 LEAD PLLC**
CASE 775−02
ISSUE E



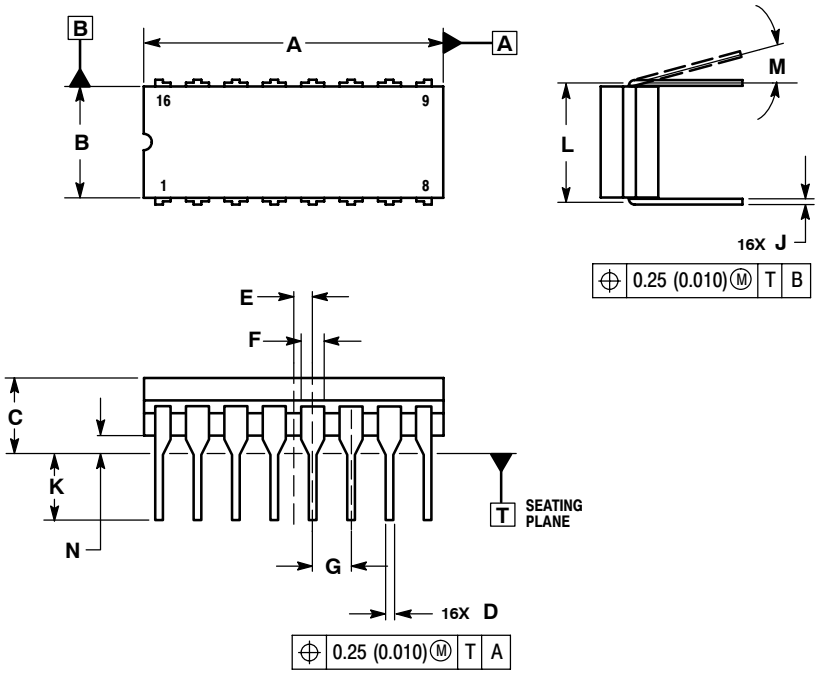




NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS IN INCHES.
3. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
4. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
5. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
6. DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.385 | 0.395 | 9.78 | 10.03 |
| B | 0.385 | 0.395 | 9.78 | 10.03 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | −−− | 0.51 | −−− |
| K | 0.025 | −−− | 0.64 | −−− |
| R | 0.350 | 0.356 | 8.89 | 9.04 |
| U | 0.350 | 0.356 | 8.89 | 9.04 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | −−− | 0.020 | −−− | 0.50 |
| Z | 2 ° | 10 ° | 2 ° | 10 ° |
| G1 | 0.310 | 0.330 | 7.88 | 8.38 |
| K1 | 0.040 | −−− | 1.02 | −−− |

## PACKAGE DIMENSIONS

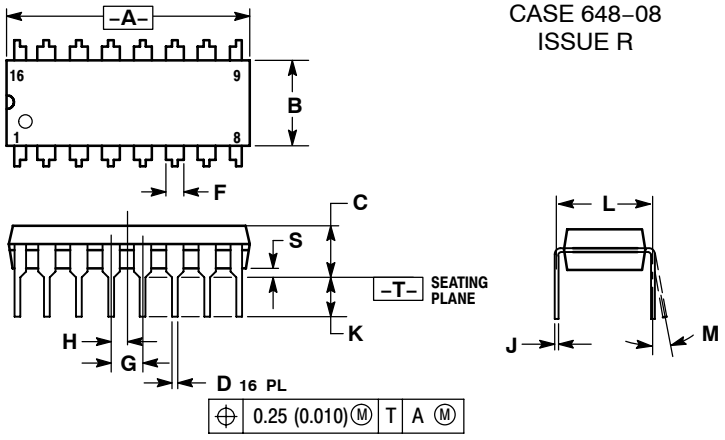
**CDIP–16**
**L SUFFIX**
CERAMIC DIP PACKAGE
CASE 620A–01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5 THIS DRAWING REPLACES OBSOLETE CASE OUTLINE 620–10.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.93 |
| B | 0.240 | 0.295 | 6.10 | 7.49 |
| C | --- | 0.200 | --- | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0 ° | 15 ° | 0 ° | 15 ° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

**PDIP–16**
**P SUFFIX**
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

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## PUBLICATION ORDERING INFORMATION

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