**Freescale Semiconductor**
**Technical Data**

Document Number: MPC875EC
Rev. 4, 08/2007

# MPC875/MPC870 PowerQUICC™ Hardware Specifications

This hardware specification contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC875/MPC870. The CPU on the MPC875/MPC870 is a 32-bit core built on Power Architecture™ technology that incorporates memory management units (MMUs) and instruction and data caches. For functional characteristics of the MPC875/MPC870, refer to the *MPC885 PowerQUICC™ Family Reference Manual*.

To locate published errata or updates for this document, refer to the MPC875/MPC870 product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

**Contents**

# 1 Overview

The MPC875/MPC870 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC875/MPC870 provides enhanced ATM functionality over that of other ATM-enabled members of the MPC860 family.

Table 1 shows the functionality supported by the MPC875/MPC870.

**Table 1. MPC875/MPC870 Devices**

| Part | Cache (Kbytes) | | Ethernet | | SCC | SMC | USB | Security Engine |
|---|---|---|---|---|---|---|---|---|
| | I Cache | D Cache | 10BaseT | 10/100 | | | | |
| MPC875 | 8 | 8 | 1 | 2 | 1 | 1 | 1 | Yes |
| MPC870 | 8 | 8 | — | 2 | — | 1 | 1 | No |

# 2 Features

The MPC875/MPC870 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC875/MPC870 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
  - The 133-MHz core frequency supports 2:1 mode only
  - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution
  - 8-Kbyte data cache and 8-Kbyte instruction cache (see Table 1)
    - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
    - Data cache is two-way, set-associative with 256 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)

- Thirty-two address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Two Fast Ethernet controllers (FEC)—Two 10/100 Mbps Ethernet/IEEE Std. 802.3® CDMA/CS that interface through MII and/or RMII interfaces
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Clock synthesizer
  - Decrementer and time base
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Security engine is optimized to handle all the algorithms associated with IPsec, SSL/TLS, SRTP, IEEE 802.11i® standard, and iSCSI processing. Available on the MPC875, the security engine contains a crypto-channel, a controller, and a set of crypto hardware accelerators (CHAs). The CHAs are:
  - Data encryption standard execution unit (DEU)
    - DES, 3DES
    - Two key (K1, K2, K1) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)
    - Implements the Rijndael symmetric key cipher

    - ECB, CBC, and counter modes
    - 128-, 192-, and 256-bit key lengths
  - Message digest execution unit (MDEU)
    - SHA with 160- or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Master/slave logic, with DMA
    - 32-bit address/32-bit data
    - Operation at MPC8xx bus frequency
  - Crypto-channel supporting multi-command descriptors
    - Integrated controller managing crypto-execution units
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Interrupts
  - Six external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Twenty-three internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Several serial DMA (SDMA) channels to support the CPM
  - Three parallel I/O registers with open-drain capability
- On-chip 16 × 16 multiply accumulate controller (MAC)
  - One operation per clock (two-clock latency, one-clock blockage)
  - MAC operates concurrently with other instructions
  - FIR loop—Four clocks per four multiplies
- Four baud-rate generators
  - Independent (can be connected to SCC or SMC)
  - Allows changes during operation
  - Autobaud support option
- SCC (serial communication controller)
  - Ethernet/IEEE 802.3® standard, supporting full 10-Mbps operation
  - HDLC/SDLC

  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support point-to-point protocol (PPP)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- SMC (serial management channel)
  - UART (low-speed operation)
  - Transparent
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loopback diagnostics)
  - USB 2.0 full-/low-speed compatible
  - The USB function mode has the following features:
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate
    - Flexible data buffers with multiple buffers per frame
    - Automatic retransmission upon transmit error
  - The USB host controller has the following features:
    - Supports control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - NRZI encoding/decoding with bit stuffing
    - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
    - Flexible data buffers with multiple buffers per frame
    - Supports local loopback mode for diagnostics (12 Mbps only)
- Serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- Inter-integrated circuit ($I^2C$) port
  - Supports master and slave modes
  - Supports a multiple-master environment

- The MPC875 has a time-slot assigner (TSA) that supports one TDM bus (TDMb)
  - Allows SCC and SMC to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - Can be internally connected to two serial channels (one SCC and one SMC)
- PCMCIA interface
  - Master (socket) interface, release 2.1-compliant
  - Supports one independent PCMCIA socket on the MPC875/MPC870
  - Eight memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: $= \neq < >$
  - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8-V core and 3.3-V I/O operation with 5-V TTL compatibility
- The MPC875/MPC870 comes in a 256-pin ball grid array (PBGA) package

The MPC875 block diagram is shown in Figure 1.

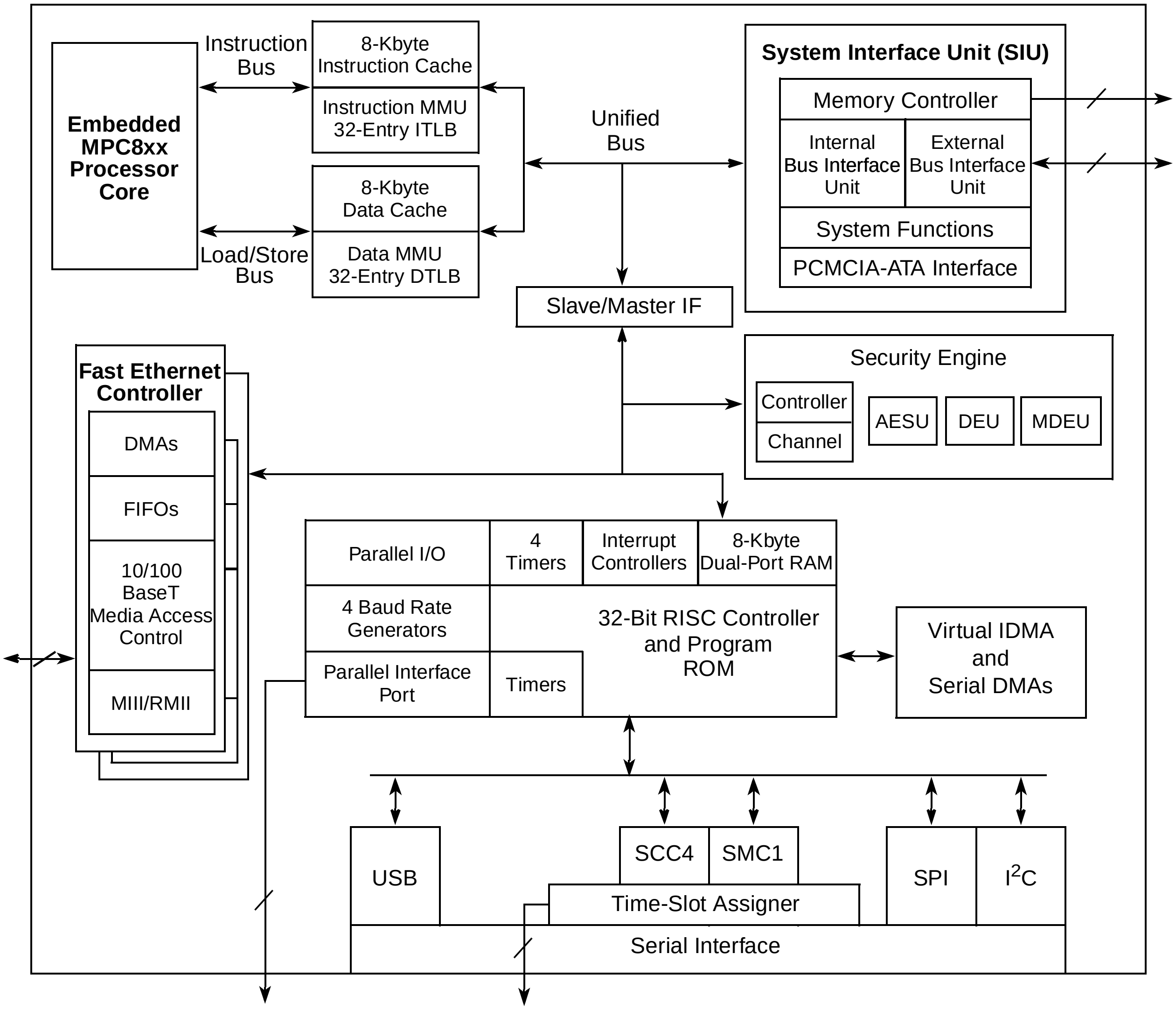


Figure 1. MPC875 Block Diagram

The MPC870 block diagram is shown in Figure 2.

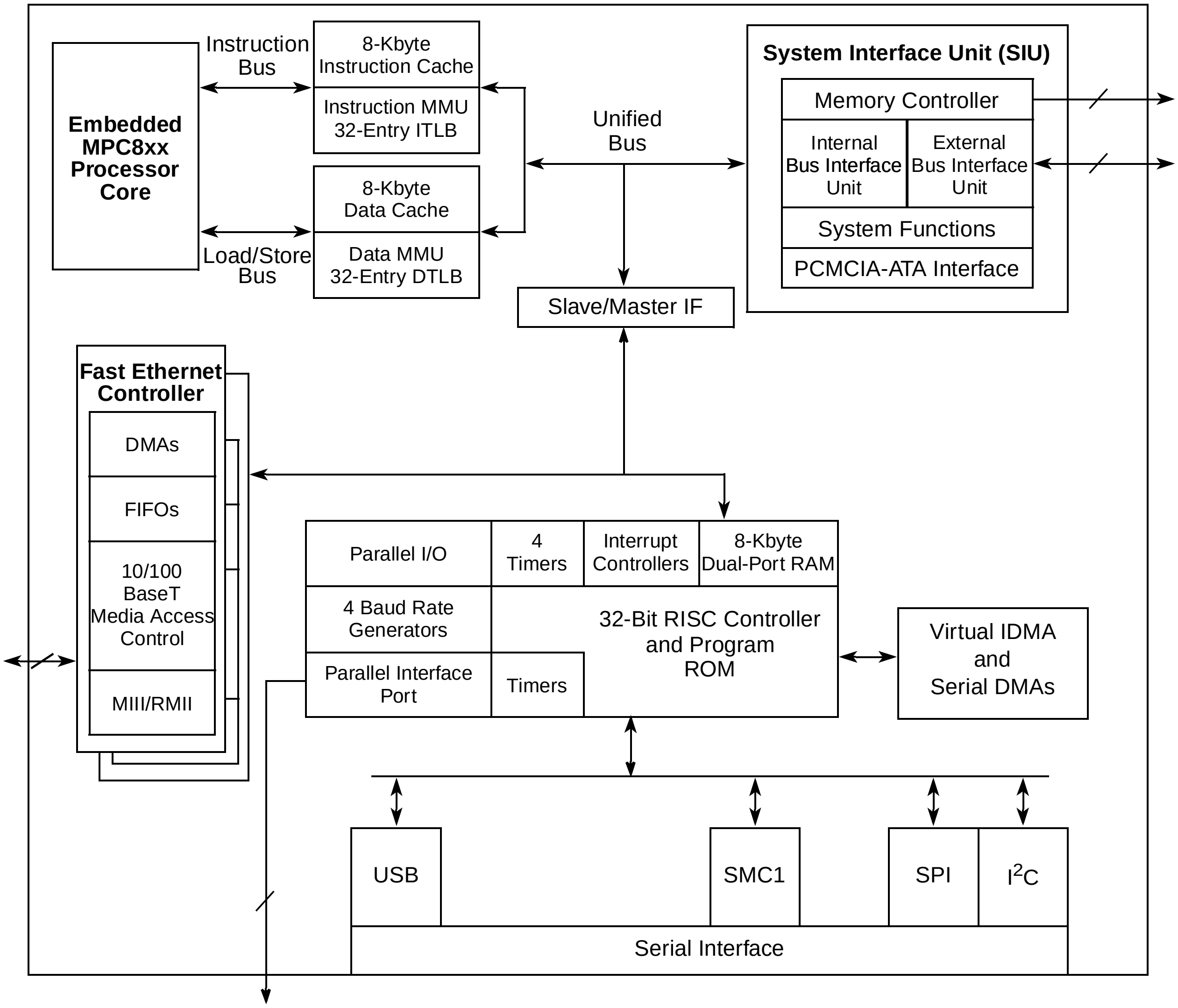


**Figure 2. MPC870 Block Diagram**

# 3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC875/MPC870. Table 2 displays the maximum tolerated ratings and Table 3 displays the operating temperatures.

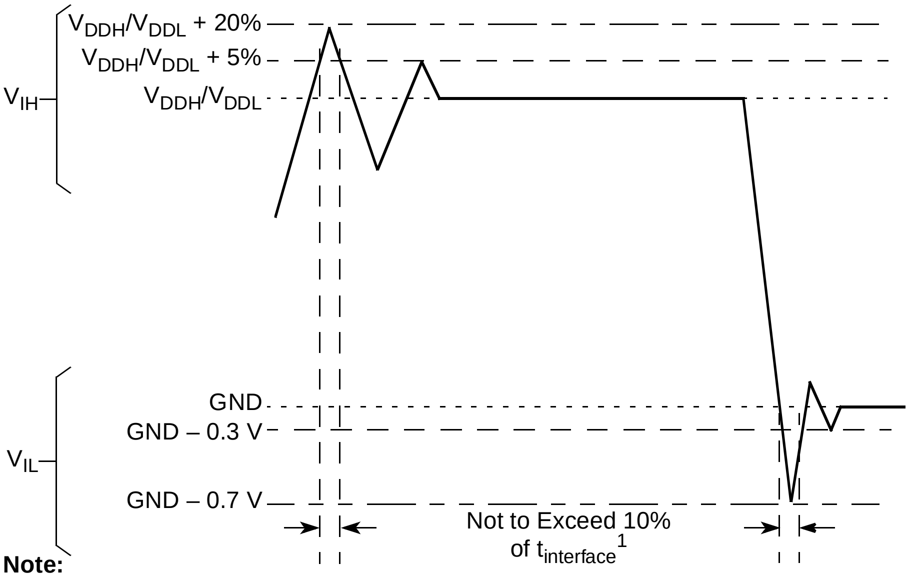
**Table 2. Maximum Tolerated Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage[1] | $V_{DDL}$ (core voltage) | –0.3 to 3.4 | V |
| | $V_{DDH}$ (I/O voltage) | –0.3 to 4 | V |
| | $V_{DDSYN}$ | –0.3 to 3.4 | V |
| | Difference between $V_{DDL}$ and $V_{DDSYN}$ | <100 | mV |
| Input voltage[2] | $V_{in}$ | GND – 0.3 to $V_{DDH}$ | V |
| Storage temperature range | $T_{stg}$ | –55 to +150 | °C |

[1] The power supply of the device must start its ramp from 0.0 V.

[2] Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
**Caution**: All inputs that tolerate 5 V cannot be more than 2.5 V greater than $V_{DDH}$. This restriction applies to power up and normal operation (that is, if the MPC875/MPC870 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the MPC875/MPC870.



**Note:**
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 3. Undershoot/Overshoot Voltage for $V_{DDH}$ and $V_{DDL}$

**Table 3. Operating Temperatures**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Temperature [1] (standard) | $T_{A(min)}$ | 0 | °C |
| | $T_{J(max)}$ | 95 | °C |
| Temperature (extended) | $T_{A(min)}$ | –40 | °C |
| | $T_{J(max)}$ | 100 | °C |

[1] Minimum temperatures are guaranteed as ambient temperature, $T_A$. Maximum temperatures are guaranteed as junction temperature, $T_J$.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{DDH}$).

# 4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC875/MPC870.

**Table 4. MPC875/MPC870 Thermal Resistance Data**

| Rating | Environment | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Junction-to-ambient[1] | Natural convection | Single-layer board (1s) | $R_{\theta JA}$[2] | 43 | °C/W |
| | | Four-layer board (2s2p) | $R_{\theta JMA}$[3] | 29 | |
| | Airflow (200 ft/min) | Single-layer board (1s) | $R_{\theta JMA}$[3] | 36 | |
| | | Four-layer board (2s2p) | $R_{\theta JMA}$[3] | 26 | |
| Junction-to-board[4] | | | $R_{\theta JB}$ | 20 | |
| Junction-to-case [5] | | | $R_{\theta JC}$ | 10 | |
| Junction-to-package top[6] | Natural convection | | $\Psi_{JT}$ | 2 | |
| | Airflow (200 ft/min) | | $\Psi_{JT}$ | 2 | |

[1] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

[2] Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

[3] Per JEDEC JESD51-6 with the board horizontal.

[4] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

[6] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

# 5 Power Dissipation

Table 5 provides information on power dissipation. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice bus speed.

**Table 5. Power Dissipation ($P_D$)**

| Die Revision | Bus Mode | Frequency | Typical[1] | Maximum[2] | Unit |
|---|---|---|---|---|---|
| 0 | 1:1 | 66 MHz | 310 | 390 | mW |
| | | 80 MHz | 350 | 430 | mW |
| | 2:1 | 133 MHz | 430 | 495 | mW |

[1] Typical power dissipation is measured at $V_{DDL}$ = $V_{DDSYN}$ = 1.8 V, and $V_{DDH}$ is at 3.3 V.

[2] Maximum power dissipation at $V_{DDL}$ = $V_{DDSYN}$ = 1.9 V, and $V_{DDH}$ is at 3.5 V.

**NOTE**

The values in Table 5 represent $V_{DDL}$-based power dissipation and do not include I/O power dissipation over $V_{DDH}$. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

The $V_{DDSYN}$ power dissipation is negligible.

# 6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC875/MPC870.

**Table 6. DC Electrical Specifications**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating voltage | $V_{DDH}$ (I/O) | 3.135 | 3.465 | V |
| | $V_{DDL}$ (core) | 1.7 | 1.9 | V |
| | $V_{DDSYN}$[1] | 1.7 | 1.9 | V |
| | Difference between $V_{DDL}$ and $V_{DDSYN}$ | — | 100 | mV |
| Input high voltage (all inputs except EXTAL and EXTCLK)[2] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage[3] | $V_{IL}$ | GND | 0.8 | V |
| EXTAL, EXTCLK input high voltage | $V_{IHC}$ | $0.7 \times V_{DDH}$ | $V_{DDH}$ | V |
| Input leakage current, $V_{in}$ = 5.5 V (except TMS, $\overline{TRST}$, DSCK, and DSDI pins) for 5-V tolerant pins[1] | $I_{in}$ | — | 100 | µA |
| Input leakage current, $V_{in}$ = $V_{DDH}$ (except TMS, $\overline{TRST}$, DSCK, and DSDI) | $I_{In}$ | — | 10 | µA |
| Input leakage current, $V_{in}$ = 0 V (except TMS, $\overline{TRST}$, DSCK, and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input capacitance[4] | $C_{in}$ | — | 20 | pF |

**Table 6. DC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Output high voltage, $I_{OH}$ = –2.0 mA, $V_{DDH}$ = 3.0 V (except XTAL and open-drain pins) | $V_{OH}$ | 2.4 | — | V |
| Output low voltage<br>$I_{OL}$ = 2.0 mA (CLKOUT)<br>$I_{OL}$ = 3.2 mA[5]<br>$I_{OL}$ = 5.3 mA[6]<br>$I_{OL}$ = 7.0 mA (TXD1/PA14, TXD2/PA12)<br>$I_{OL}$ = 8.9 mA ($\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$) | $V_{OL}$ | — | 0.5 | V |

[1] The difference between $V_{DDL}$ and $V_{DDSYN}$ cannot be more than 100 mV.

[2] The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], PE(14:31), TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII1_TXEN, and MII_MDIO are 5-V tolerant. The minimum voltage is still 2.0 V.

[3] $V_{IL}$(max) for the $I^2C$ interface is 0.8 V rather than the 1.5 V as specified in the $I^2C$ standard.

[4] Input capacitance is periodically sampled.

[5] A(0:31), TSIZ0/$\overline{\text{REG}}$, TSIZ1, D(0:31), $\overline{\text{IRQ}}$(2:4), $\overline{\text{IRQ6}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, IP_B(0:1), PA(0:4), PA(6:7), PA(10:11), PA15, PB19, PB(23:31), PC(6:7), PC(10:13), PC15, PD8, PE(14:31), MII1_CRS, MII_MDIO, MII1_TXEN, and MII1_COL.

[6] $\overline{\text{BDIP}}$/$\overline{\text{GPL\_B}}$(5), $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ/$\overline{\text{IRQ6}}$, $\overline{\text{CS}}$(0:7), $\overline{\text{WE}}$(0:3), $\overline{\text{BS}}$_A(0:3), $\overline{\text{GPL\_A0}}$/$\overline{\text{GPL\_B0}}$, $\overline{\text{OE}}$/$\overline{\text{GPL\_A1}}$/$\overline{\text{GPL\_B1}}$, $\overline{\text{GPL\_A}}$(2:3)/$\overline{\text{GPL\_B}}$(2:3)/$\overline{\text{CS}}$(2:3), UPWAITA/$\overline{\text{GPL\_A4}}$, UPWAITB/$\overline{\text{GPL\_B4}}$, $\overline{\text{GPL\_A5}}$, ALE_A, $\overline{\text{CE1}}$_A, $\overline{\text{CE2}}$_A, OP(0:3), and BADDR(28:30).

# 7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

**NOTE**

The $V_{DDSYN}$ power dissipation is negligible.

## 7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$ = ambient temperature (°C)
$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)
$P_D$ = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

## 7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

$T_B$ = board temperature (°C)

$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

## 7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

## 7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$ = thermal characterization parameter
$T_T$ = thermocouple temperature on top of package
$P_D$ = power dissipation in package

The thermal characterization parameter is measured per the JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

## 7.6 References

| | |
|---|---|
| Semiconductor Equipment and Materials International<br>805 East Middlefield Rd<br>Mountain View, CA 94043 | (415) 964-5111 |
| MIL-SPEC and EIA/JESD (JEDEC) specifications<br>(Available from Global Engineering Documents) | 800-854-7179 or<br>303-397-7956 |
| JEDEC Specifications | http://www.jedec.org |

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. 2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

# 8 Power Supply and Power Sequencing

This section provides design considerations for the MPC875/MPC870 power supply. The MPC875/MPC870 has a core voltage ($V_{DDL}$) and PLL voltage ($V_{DDSYN}$), which both operate at a lower voltage than the I/O voltage ($V_{DDH}$). The I/O section of the MPC875/MPC870 is supplied with 3.3 V across $V_{DDH}$ and $V_{SS}$ (GND).

The signals PA[0:3], PA[8:11], PB15, PB[24:25], PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. No input can be more than 2.5 V greater than $V_{DDH}$. In addition, 5-V tolerant pins cannot exceed 5.5 V, and remaining input pins cannot exceed 3.465 V. This restriction applies to power up, power down, and normal operation.

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- $V_{DDL}$ must not exceed $V_{DDH}$ during power up and power down
- $V_{DDL}$ must not exceed 1.9 V, and $V_{DDH}$ must not exceed 3.465 V

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 4 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.

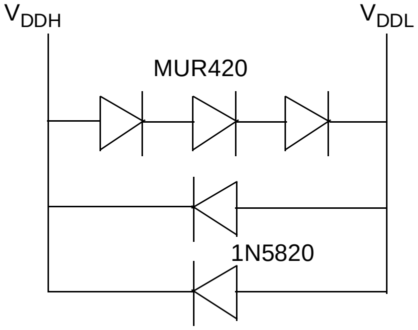


**Figure 4. Example Voltage Sequencing Circuit**

# 9 Mandatory Reset Configurations

The MPC875/MPC870 requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, the HRCW[DBGC] value needs to be set to binary X1 in the HRCW and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset. This can be done by asserting the $\overline{\text{RSTCONF}}$ during $\overline{\text{HRESET}}$ assertion.

If HRCW is disabled, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion.

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR need to be configured with the mandatory values in Table 7 in the boot code after the reset is negated.

**Table 7. Mandatory Reset Configuration of MPC875/MPC870**

| Register/Configuration | Field | Value (Binary) |
|---|---|---|
| HRCW (Hardware reset configuration word) | HRCW[DBGC] | X1 |
| SIUMCR (SIU module configuration register) | SIUMCR[DBGC] | X1 |
| MBMR (Machine B mode register) | MBMR[GPLB4DIS} | 0 |
| PAPAR (Port A pin assignment register) | PAPAR[5:9]<br>PAPAR[12:13] | 0 |

**Table 7. Mandatory Reset Configuration of MPC875/MPC870 (continued)**

| Register/Configuration | Field | Value (Binary) |
|---|---|---|
| PADIR (Port A data direction register) | PADIR[5:9]<br>PADIR[12:13] | 0 |
| PBPAR (Port B pin assignment register) | PBPAR[14:18]<br>PBPAR[20:22] | 0 |
| PBDIR (Port B data direction register) | PBDIR[14:8]<br>PBDIR[20:22] | 0 |
| PCPAR (Port C pin assignment register) | PCPAR[4:5]<br>PCPAR[8:9]<br>PCPAR[14] | 0 |
| PCDIR (Port C data direction register) | PCDIR[4:5]<br>PCDIR[8:9]<br>PCDIR[14] | 0 |
| PDPAR (Port D pin assignment register) | PDPAR[3:7]<br>PDPAR[9:5] | 0 |
| PDDIR (Port D data direction register) | PDDIR[3:7]<br>PDDIR[9:15] | 0 |

# 10 Layout Practices

Each $V_{DD}$ pin on the MPC875/MPC870 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{DD}$ power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip $V_{DD}$ and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as $V_{DD}$ and GND planes should be used.

All output pins on the MPC875/MPC870 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{DD}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, refer to Section 14.4.3, "Clock Synthesizer Power ($V_{DDSYN}$, $V_{SSSYN}$, $V_{SSSYN1}$)," in the *MPC885 PowerQUICC™ Family Reference Manual*.

# 11 Bus Signal Timing

The maximum bus speed supported by the MPC875/MPC870 is 80 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC875/MPC870 used at 133 MHz must be configured for a 66 MHz bus). Table 8 shows the frequency ranges for standard part frequencies in 1:1 bus mode, and Table 9 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

**Table 8. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)**

| Part Frequency | 66 MHz | | 80 MHz | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| Core frequency | 40 | 66.67 | 40 | 80 |
| Bus frequency | 40 | 66.67 | 40 | 80 |

**Table 9. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)**

| Part Frequency | 66 MHz | | 80 MHz | | 133 MHz | |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max |
| Core frequency | 40 | 66.67 | 40 | 80 | 40 | 133 |
| Bus frequency | 20 | 33.33 | 20 | 40 | 20 | 66 |

Table 10 provides the bus operation timing for the MPC875/MPC870 at 33, 40, 66, and 80 MHz.

The timing for the MPC875/MPC870 bus shown Table 10, assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

**Table 10. Bus Operation Timings**

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B1 | Bus period (CLKOUT), see Table 8 | — | — | — | — | — | — | — | — | ns |
| B1a | EXTCLK to CLKOUT phase skew—If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew. | –2 | +2 | –2 | +2 | –2 | +2 | –2 | +2 | ns |
| B1b | CLKOUT frequency jitter peak-to-peak | — | 1 | — | 1 | — | 1 | — | 1 | ns |
| B1c | Frequency jitter on EXTCLK | — | 0.50 | — | 0.50 | — | 0.50 | — | 0.50 | % |
| B1d | CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz | — | 4 | — | 4 | — | 4 | — | 4 | ns |
| | CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz | — | 5 | — | 5 | — | 5 | — | 5 | ns |

## Table 10. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B2 | CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1) | 12.1 | 18.2 | 10.0 | 15.0 | 6.1 | 9.1 | 5.0 | 7.5 | ns |
| B3 | CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1) | 12.1 | 18.2 | 10.0 | 15.0 | 6.1 | 9.1 | 5.0 | 7.5 | ns |
| B4 | CLKOUT rise time | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B5 | CLKOUT fall time | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B7 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, D(0:31) output hold (MIN = 0.25 × B1) | 7.60 | — | 6.30 | — | 3.80 | — | 3.13 | — | ns |
| B7a | CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, $\overline{\text{BDIP}}$, PTR output hold (MIN = 0.25 × B1) | 7.60 | — | 6.30 | — | 3.80 | — | 3.13 | — | ns |
| B7b | CLKOUT to $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{\text{STS}}$ output hold (MIN = 0.25 × B1) | 7.60 | — | 6.30 | — | 3.80 | — | 3.13 | — | ns |
| B8 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, D(0:31) valid (MAX = 0.25 × B1 + 6.3) | — | 13.80 | — | 12.50 | — | 10.00 | — | 9.43 | ns |
| B8a | CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, $\overline{\text{BDIP}}$, PTR valid (MAX = 0.25 × B1 + 6.3) | — | 13.80 | — | 12.50 | — | 10.00 | — | 9.43 | ns |
| B8b | CLKOUT to $\overline{\text{BR}}$, $\overline{\text{BG}}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{\text{STS}}$ valid [2] (MAX = 0.25 × B1 + 6.3) | — | 13.80 | — | 12.50 | — | 10.00 | — | 9.43 | ns |
| B9 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, D(0:31), TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, PTR High-Z (MAX = 0.25 × B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.43 | ns |
| B11 | CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ assertion (MAX = 0.25 × B1 + 6.0) | 7.60 | 13.60 | 6.30 | 12.30 | 3.80 | 9.80 | 3.13 | 9.13 | ns |
| B11a | CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30[1]) | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.80 | 2.5 | 9.3 | ns |
| B12 | CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ negation (MAX = 0.25 × B1 + 4.8) | 7.60 | 12.30 | 6.30 | 11.00 | 3.80 | 8.50 | 3.13 | 7.92 | ns |
| B12a | CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.5 | 9.00 | ns |
| B13 | CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ High-Z (MIN = 0.25 × B1) | 7.60 | 21.60 | 6.30 | 20.30 | 3.80 | 14.00 | 3.13 | 12.93 | ns |
| B13a | CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.5 | 15.00 | ns |
| B14 | CLKOUT to $\overline{\text{TEA}}$ assertion (MAX = 0.00 × B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | ns |

## Table 10. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B15 | CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 × B1 + 2.50) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | ns |
| B16 | $\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6 | — | ns |
| B16a | $\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5) | 4.50 | — | 4.50 | — | 4.50 | — | 4.50 | — | ns |
| B16b | $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time)[2] (4MIN = 0.00 × B1 + 0.00) | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | — | ns |
| B17 | CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = 0.00 × B1 + 1.00[3]) | 1.00 | — | 1.00 | — | 2.00 | — | 2.00 | — | ns |
| B17a | CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B18 | D(0:31) valid to CLKOUT rising edge (setup time)[4] (MIN = 0.00 × B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B19 | CLKOUT rising edge to D(0:31) valid (hold time)[4] (MIN = 0.00 × B1 + 1.00[5]) | 1.00 | — | 1.00 | — | 2.00 | — | 2.00 | — | ns |
| B20 | D(0:31) valid to CLKOUT falling edge (setup time)[6] (MIN = 0.00 × B1 + 4.00) | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | — | ns |
| B21 | CLKOUT falling edge to D(0:31) valid (hold time)[6] (MIN = 0.00 × B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B22 | CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.43 | ns |
| B22a | CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 × B1 + 8.00) | — | 8.00 | — | 8.00 | — | 8.00 | — | 8.00 | ns |
| B22b | CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 × B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.43 | ns |
| B22c | CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 × B1 + 6.6) | 10.90 | 18.00 | 10.90 | 16.00 | 5.20 | 12.30 | 4.69 | 10.93 | ns |
| B23 | CLKOUT rising edge to $\overline{\text{CS}}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 and CSNT = 0 (MAX = 0.00 × B1 + 8.00) | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | ns |
| B24 | A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B24a | A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0 (MIN = 0.50 × B1 – 2.00) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |

### Table 10. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B25 | CLKOUT rising edge to $\overline{\text{OE}}$, $\overline{\text{WE}}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00) | — | 9.00 | | 9.00 | | 9.00 | — | 9.00 | ns |
| B26 | CLKOUT rising edge to $\overline{\text{OE}}$ negated (MAX = 0.00 × B1 + 9.00) | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | ns |
| B27 | A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00) | 35.90 | — | 29.30 | — | 16.90 | — | 13.60 | — | ns |
| B27a | A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00) | 43.50 | — | 35.50 | — | 20.70 | — | 16.75 | — | ns |
| B28 | CLKOUT rising edge to $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00) | — | 9.00 | — | 9.00 | — | 9.00 | — | 9.00 | ns |
| B28a | CLKOUT falling edge to $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 9.93 | ns |
| B28b | CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80) | — | 14.30 | — | 13.00 | — | 10.50 | — | 9.93 | ns |
| B28c | CLKOUT falling edge to $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6) | 10.90 | 18.00 | 10.90 | 18.00 | 5.20 | 12.30 | 4.69 | 11.29 | ns |
| B28d | CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6) | — | 18.00 | — | 18.00 | — | 12.30 | — | 11.30 | ns |
| B29 | $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B29a | $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B29b | $\overline{\text{CS}}$ negated to D(0:31) High-Z GPCM write access, ACS = 00, TRLX = 0 and CSNT = 0 (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B29c | $\overline{\text{CS}}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |

## Table 10. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B29d | $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00) | 43.50 | — | 35.50 | — | 20.70 | — | 16.75 | — | ns |
| B29e | $\overline{\text{CS}}$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MIN = 1.50 × B1 – 2.00) | 43.50 | — | 35.50 | — | 20.70 | — | 16.75 | — | ns |
| B29f | $\overline{\text{WE}}$(0:3/BS_B[0:3]) negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7] | 5.00 | — | 3.00 | — | 0.00 | — | 0.00 | — | ns |
| B29g | $\overline{\text{CS}}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7] | 5.00 | — | 3.00 | — | 0.00 | — | 0.00 | — | ns |
| B29h | $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 3.30) | 38.40 | — | 31.10 | — | 17.50 | — | 13.85 | — | ns |
| B29i | $\overline{\text{CS}}$ negated to D(0:31) (0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 3.30) | 38.40 | — | 31.10 | — | 17.50 | — | 13.85 | — | ns |
| B30 | $\overline{\text{CS}}$, $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access[8] (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B30a | $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A(0:31), invalid GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS == 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B30b | $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated to A(0:31), invalid GPCM BADDR(28:30), invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{\text{CS}}$ negated to A(0:31), invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS == 11, EBDF = 0 (MIN = 1.50 × B1 – 2.00) | 43.50 | — | 35.50 | — | 20.70 | — | 16.75 | — | ns |
| B30c | $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS == 11, EBDF = 1 (MIN = 0.375 × B1 – 3.00) | 8.40 | — | 6.40 | — | 2.70 | — | 1.70 | — | ns |

### Table 10. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B30d | $\overline{\text{WE}}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{\text{CS}}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1 | 38.67 | — | 31.38 | — | 17.83 | — | 14.19 | — | ns |
| B31 | CLKOUT falling edge to $\overline{\text{CS}}$ valid as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B31a | CLKOUT falling edge to $\overline{\text{CS}}$ valid as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 10.00 | ns |
| B31b | CLKOUT rising edge to $\overline{\text{CS}}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00) | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B31c | CLKOUT rising edge to $\overline{\text{CS}}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.30) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.40 | ns |
| B31d | CLKOUT falling edge to $\overline{\text{CS}}$ valid as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6) | 13.30 | 18.00 | 11.30 | 16.00 | 7.60 | 12.30 | 4.69 | 11.30 | ns |
| B32 | CLKOUT falling edge to $\overline{\text{BS}}$ valid as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B32a | CLKOUT falling edge to $\overline{\text{BS}}$ valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 10.00 | ns |
| B32b | CLKOUT rising edge to $\overline{\text{BS}}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00) | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B32c | CLKOUT rising edge to $\overline{\text{BS}}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 10.00 | ns |
| B32d | CLKOUT falling edge to $\overline{\text{BS}}$ valid as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60) | 13.30 | 18.00 | 11.30 | 16.00 | 7.60 | 12.30 | 4.49 | 11.30 | ns |
| B33 | CLKOUT falling edge to $\overline{\text{GPL}}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |

**Table 10. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B33a | CLKOUT rising edge to $\overline{\text{GPL}}$ valid as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 10.00 | ns |
| B34 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B34a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B34b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 – 2.00) | 20.70 | — | 16.70 | — | 9.40 | — | 6.80 | — | ns |
| B35 | A(0:31), BADDR(28:30) to $\overline{\text{CS}}$ valid as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B35a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid as requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B35b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{BS}}$ valid as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00) | 20.70 | — | 16.70 | — | 9.40 | — | 7.40 | — | ns |
| B36 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{GPL}}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B37 | UPWAIT valid to CLKOUT falling edge[9] (MIN = 0.00 × B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B38 | CLKOUT falling edge to UPWAIT valid[9] (MIN = 0.00 × B1 + 1.00) | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| B39 | $\overline{\text{AS}}$ valid to CLKOUT rising edge[10] (MIN = 0.00 × B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B40 | A(0:31), TSIZ(0:1), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$ valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B41 | $\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |

### Table 10. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B42 | CLKOUT rising edge to $\overline{\text{TS}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B43 | $\overline{\text{AS}}$ negation to memory controller signals negation (MAX = TBD) | — | TBD | — | TBD | — | TBD | — | TBD | ns |

[1] For part speeds above 50 MHz, use 9.80 ns for B11a.

[2] The timing required for $\overline{\text{BR}}$ input is relevant when the MPC875/MPC870 is selected to work with the internal bus arbiter. The timing for $\overline{\text{BG}}$ input is relevant when the MPC875/MPC870 is selected to work with the external bus arbiter.

[3] For part speeds above 50 MHz, use 2 ns for B17.

[4] The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{\text{TA}}$ input signal is asserted.

[5] For part speeds above 50 MHz, use 2 ns for B19.

[6] The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

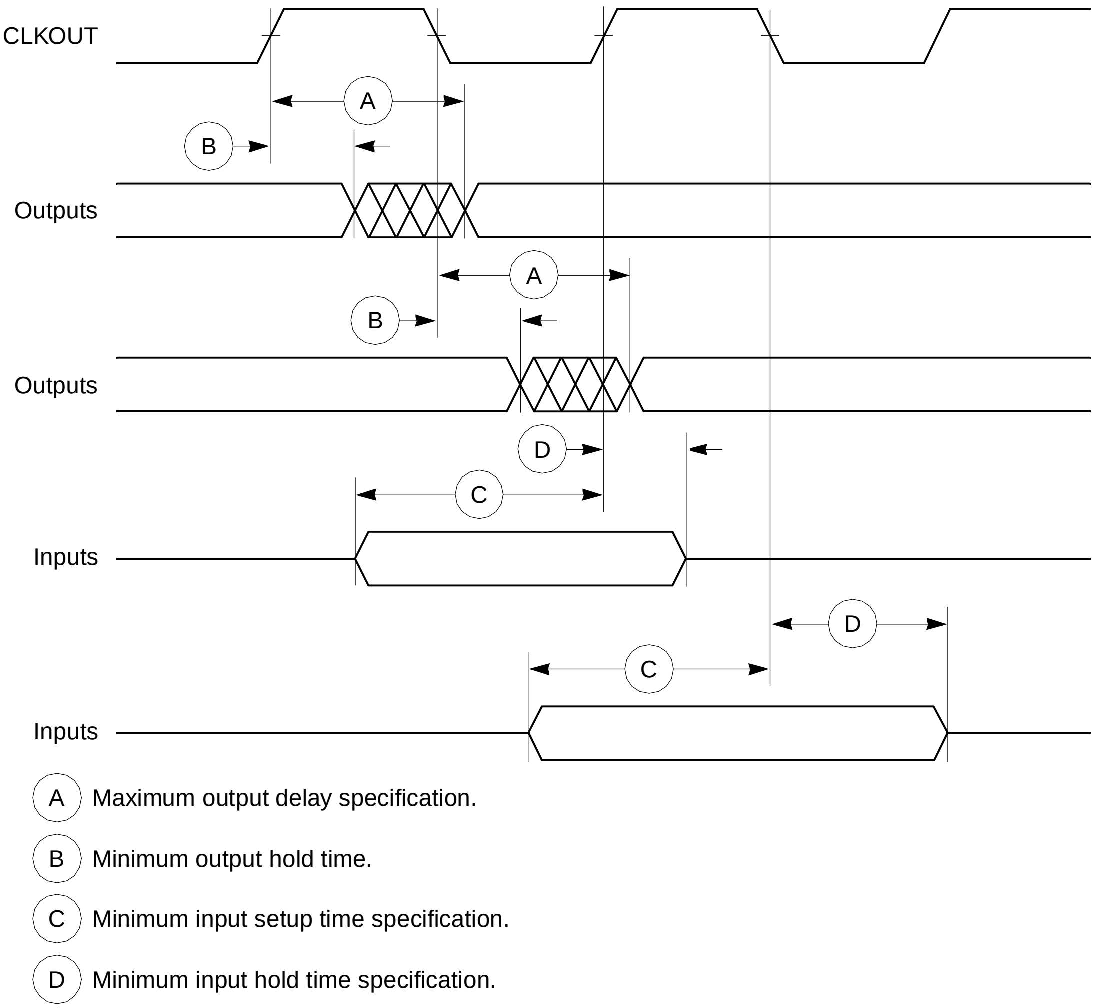
[7] This formula applies to bus operation up to 50 MHz.

[8] The timing B30 refers to $\overline{\text{CS}}$ when ACS = 00 and to $\overline{\text{WE}}$(0:3) when CSNT = 0.

[9] The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 20.

[10] The $\overline{\text{AS}}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 23.

Figure 5 provides the control timing diagram.



A Maximum output delay specification.

B Minimum output hold time.

C Minimum input setup time specification.

D Minimum input hold time specification.

**Figure 5. Control Timing**

Figure 6 provides the timing for the external clock.

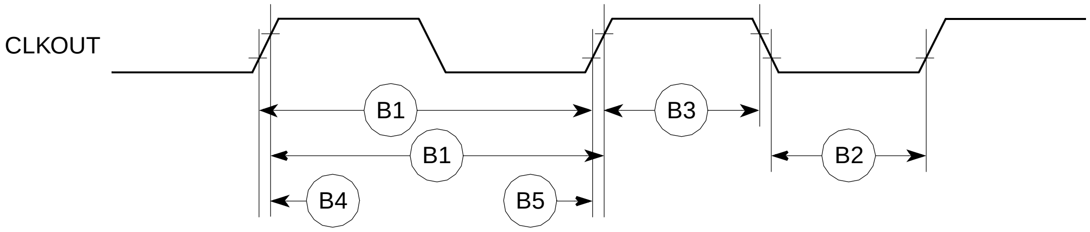


**Figure 6. External Clock Timing**

Figure 7 provides the timing for the synchronous output signals.

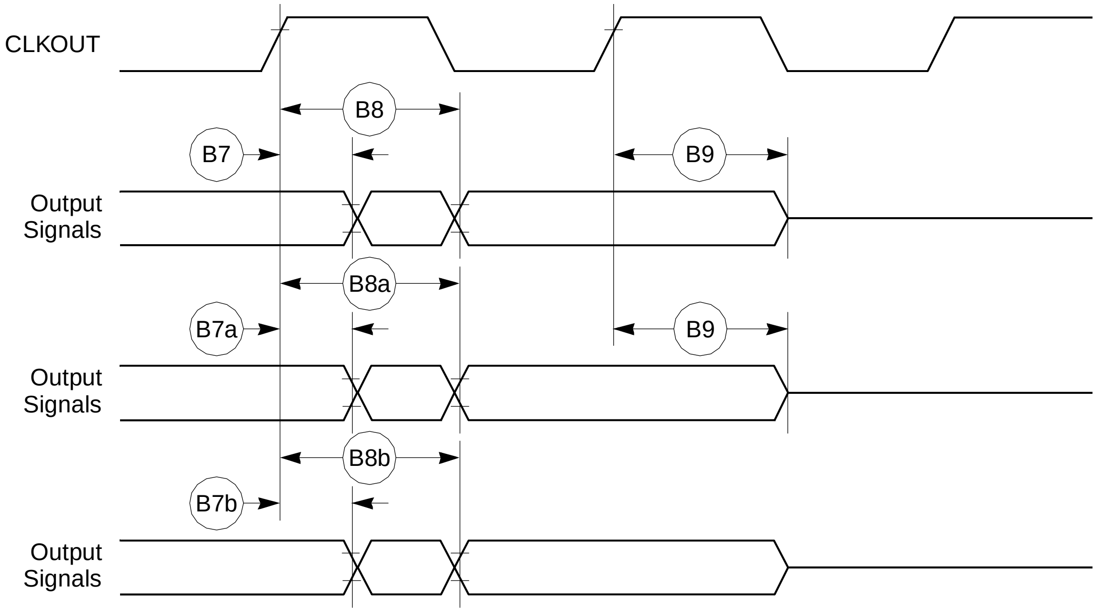


Figure 7. Synchronous Output Signals Timing

Figure 8 provides the timing for the synchronous active pull-up and open-drain output signals.

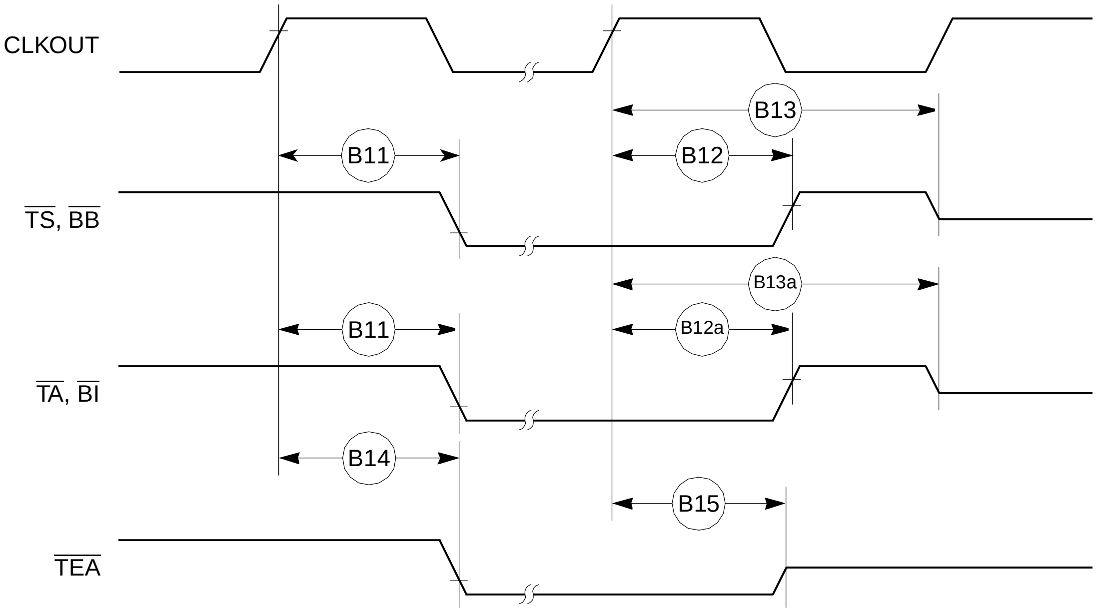


Figure 8. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 9 provides the timing for the synchronous input signals.

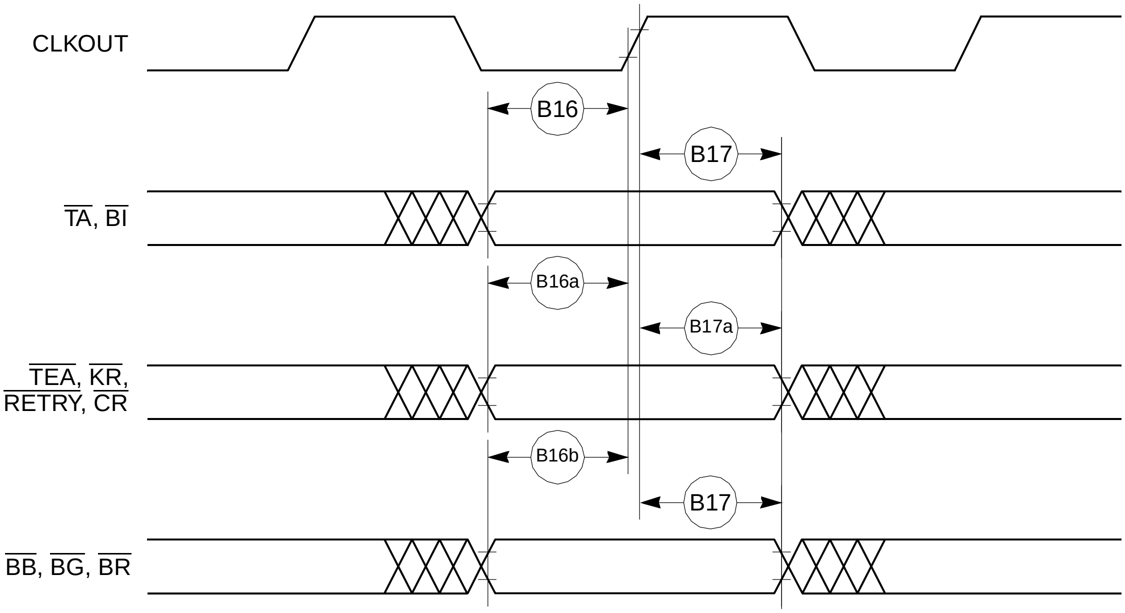


Figure 9. Synchronous Input Signals Timing

Figure 10 provides normal case timing for input data. It also applies to normal read accesses under the control of the user-programmable machine (UPM) in the memory controller.

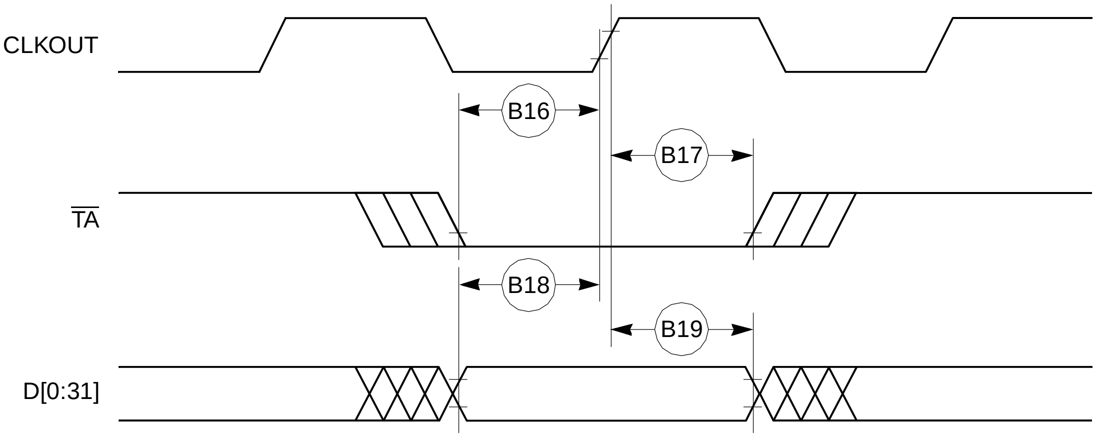


Figure 10. Input Data Timing in Normal Case

Figure 11 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

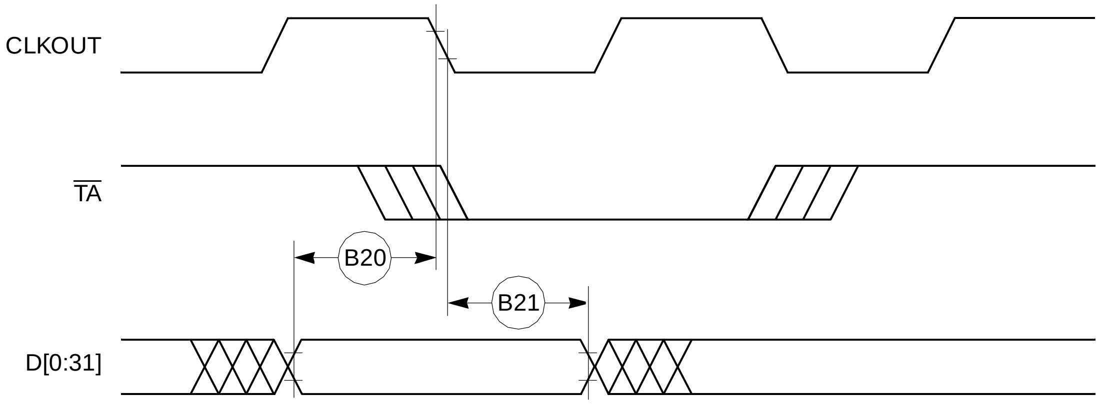


**Figure 11. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1**

Figure 12 through Figure 15 provide the timing for the external bus read controlled by various GPCM factors.

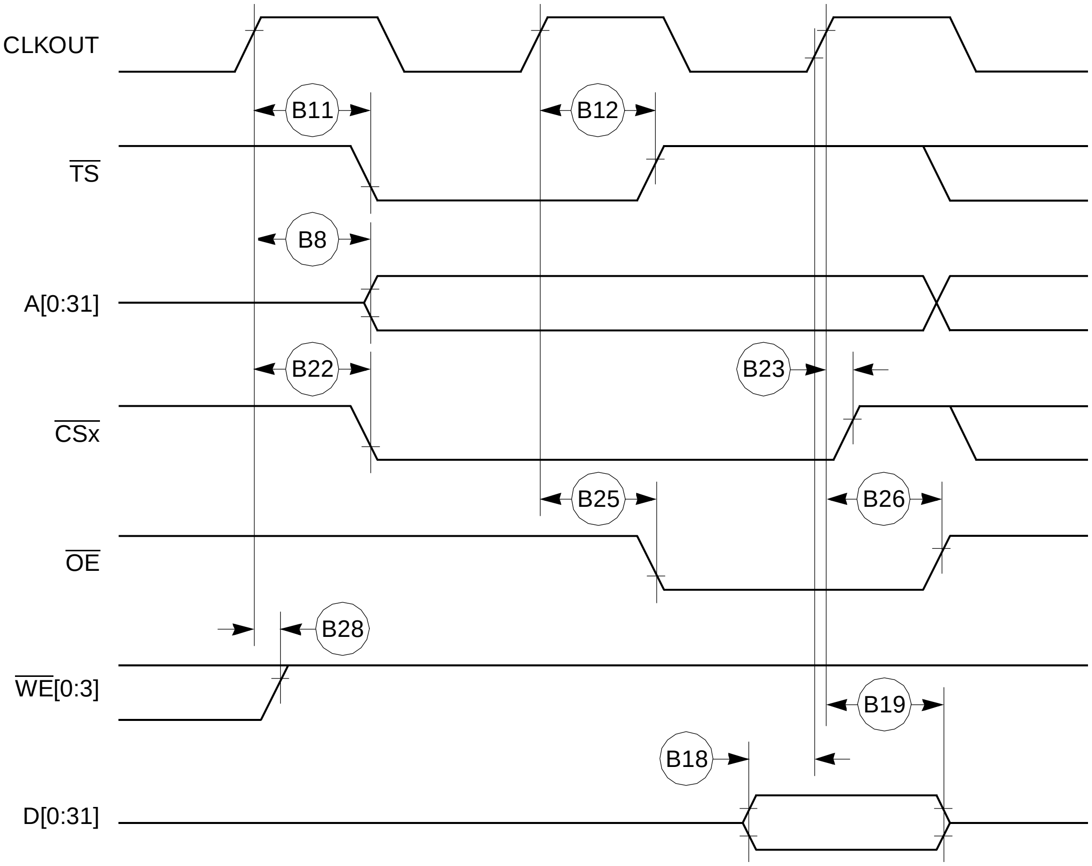


**Figure 12. External Bus Read Timing (GPCM Controlled—ACS = 00)**

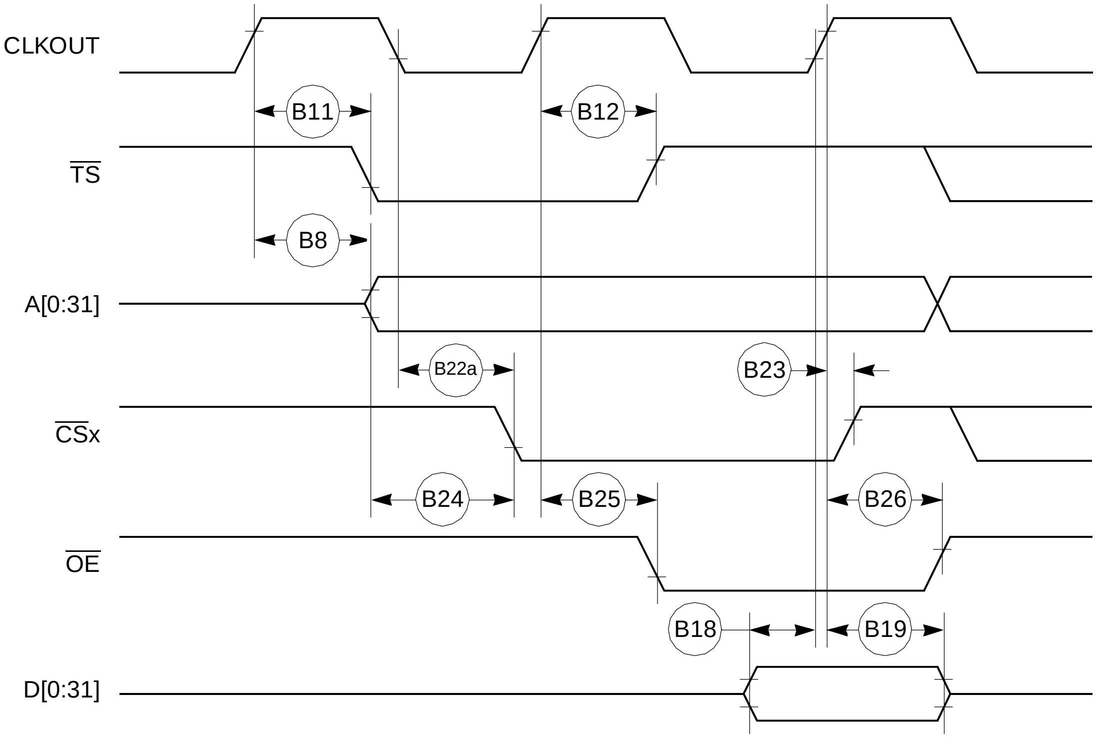


**Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)**

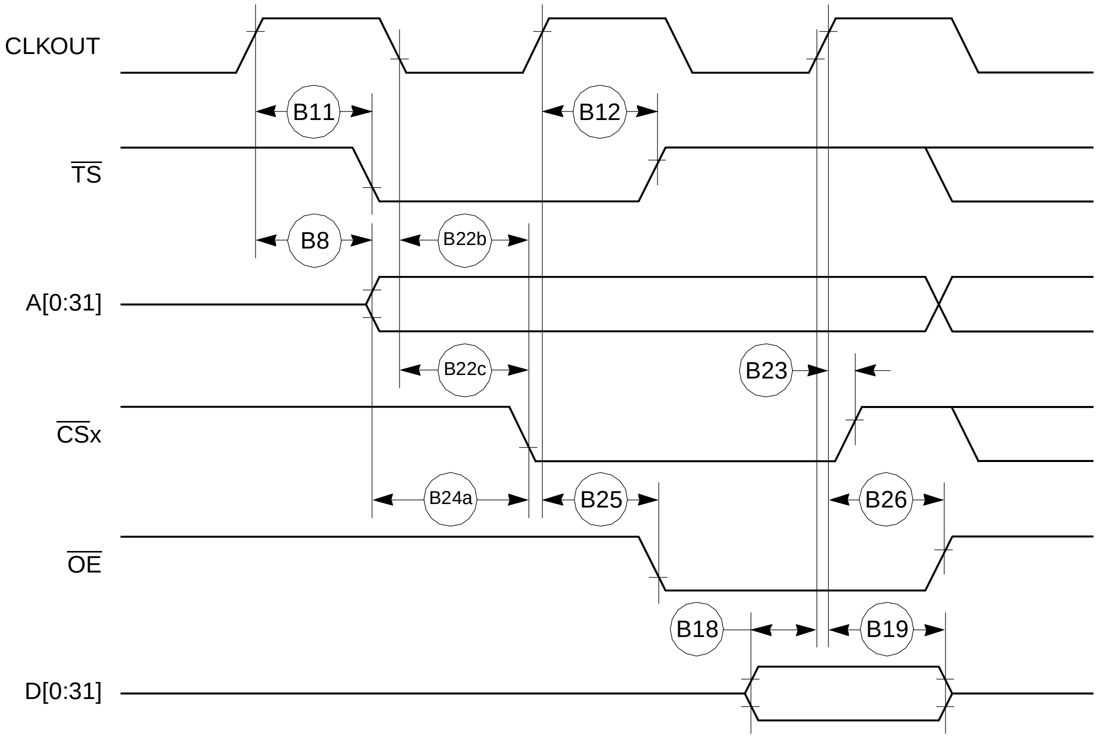


**Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)**

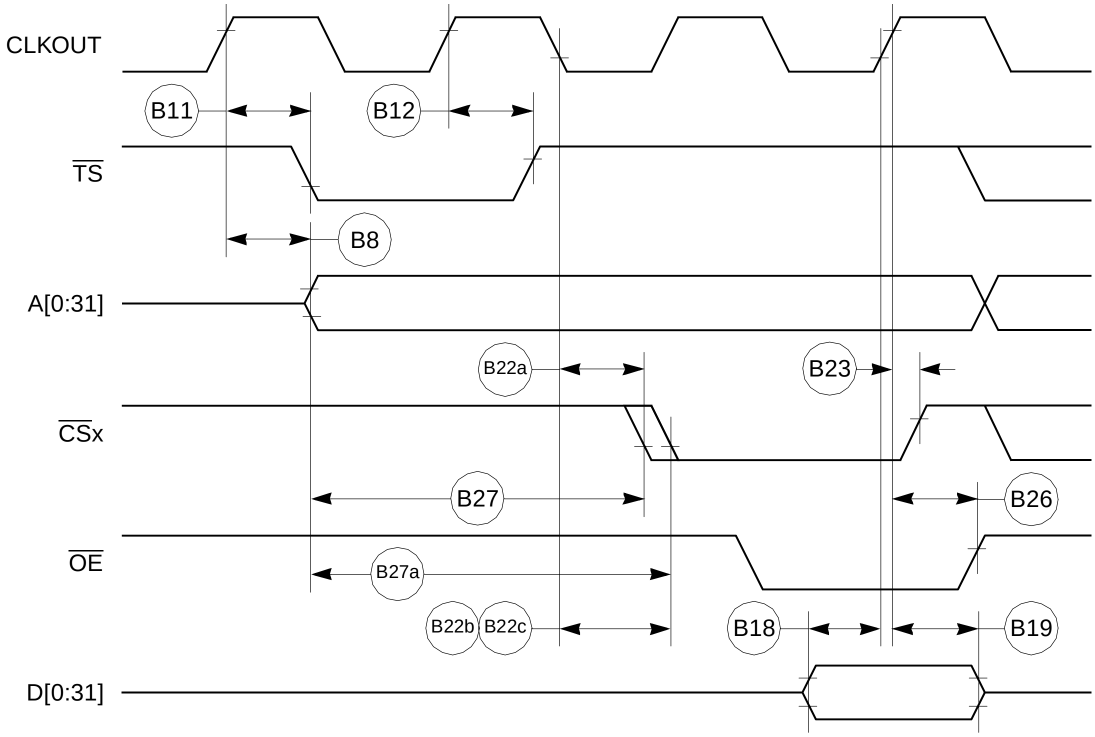


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 16 through Figure 18 provide the timing for the external bus write controlled by various GPCM factors.

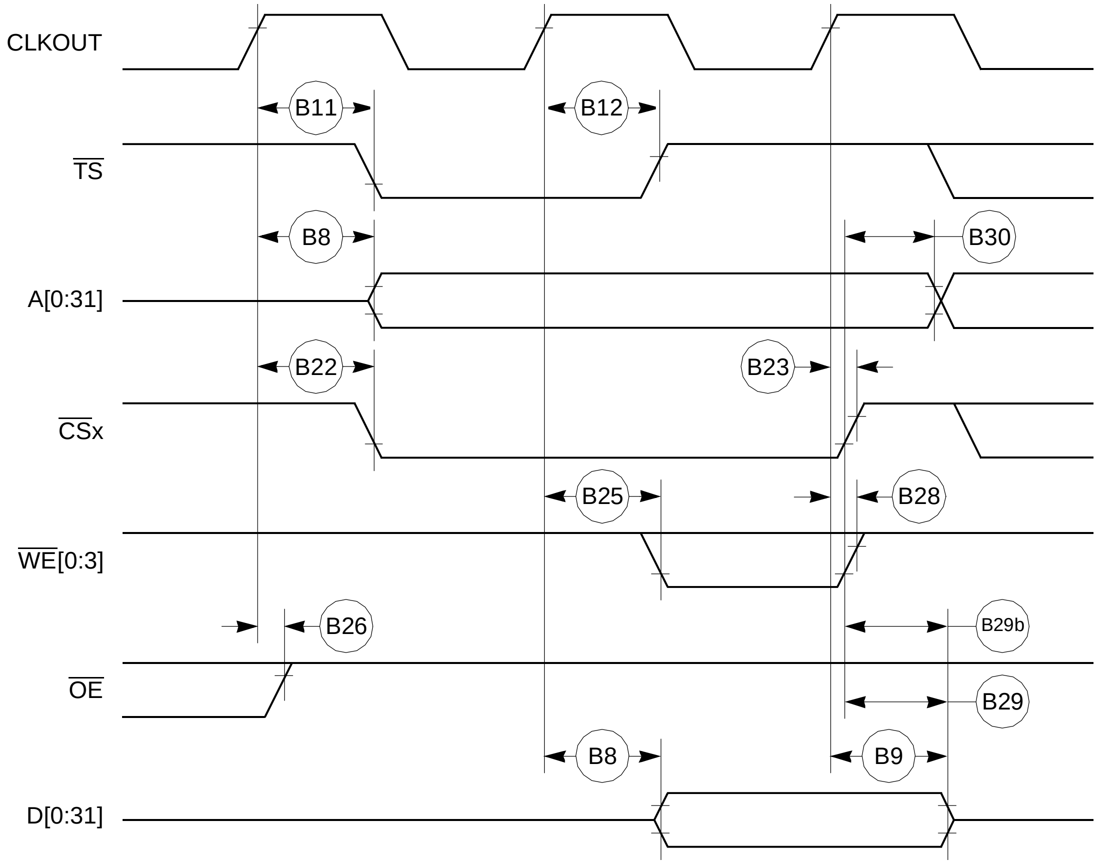


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

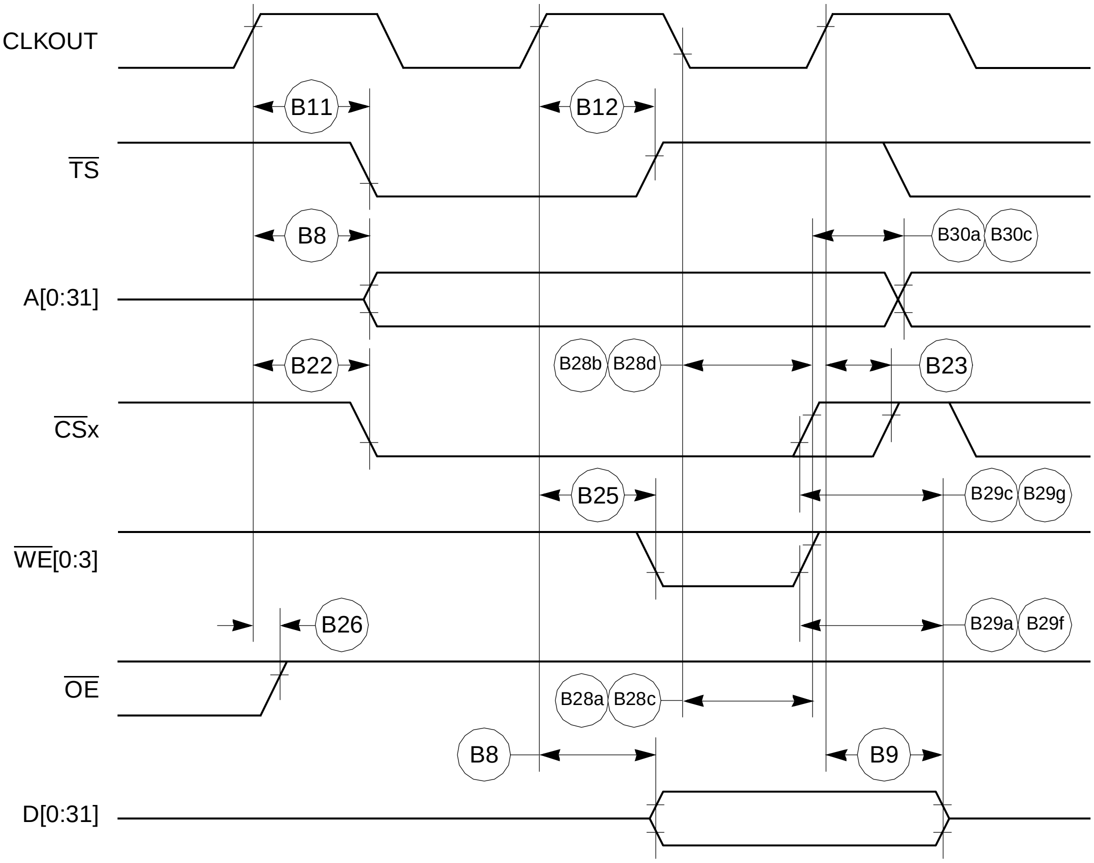


Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

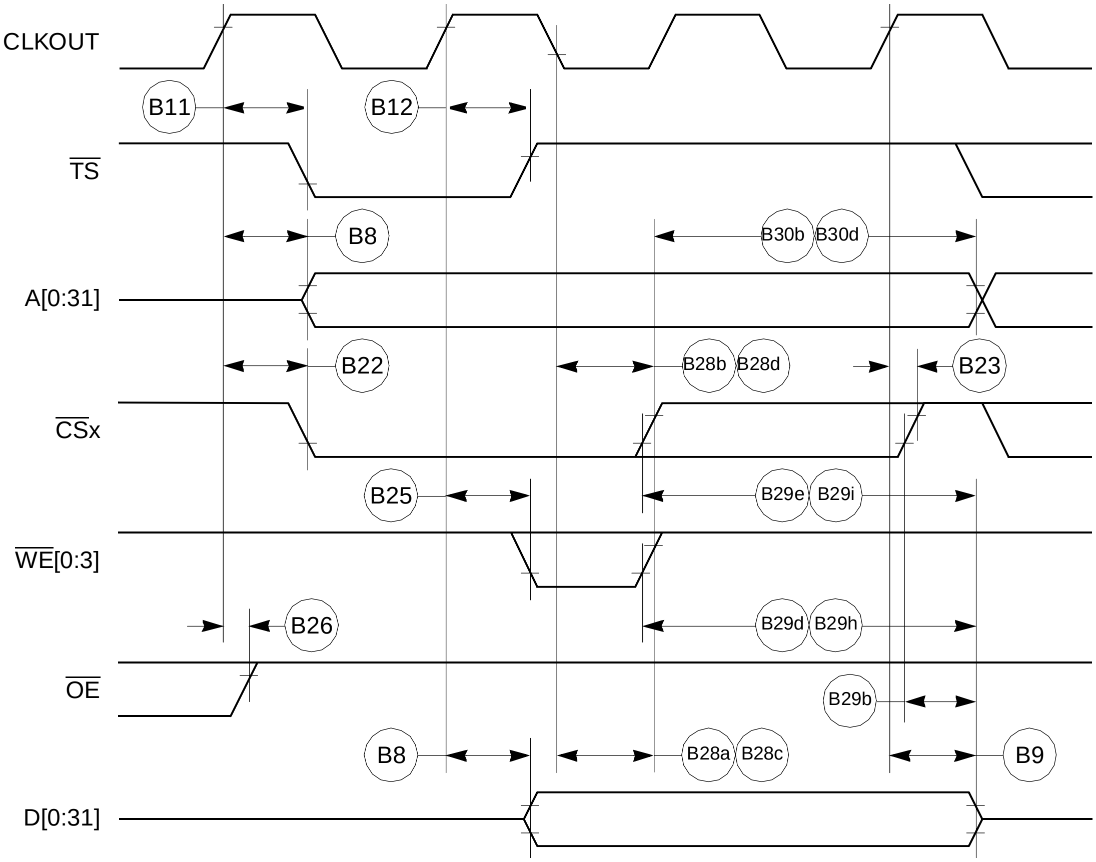


**Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)**

Figure 19 provides the timing for the external bus controlled by the UPM.

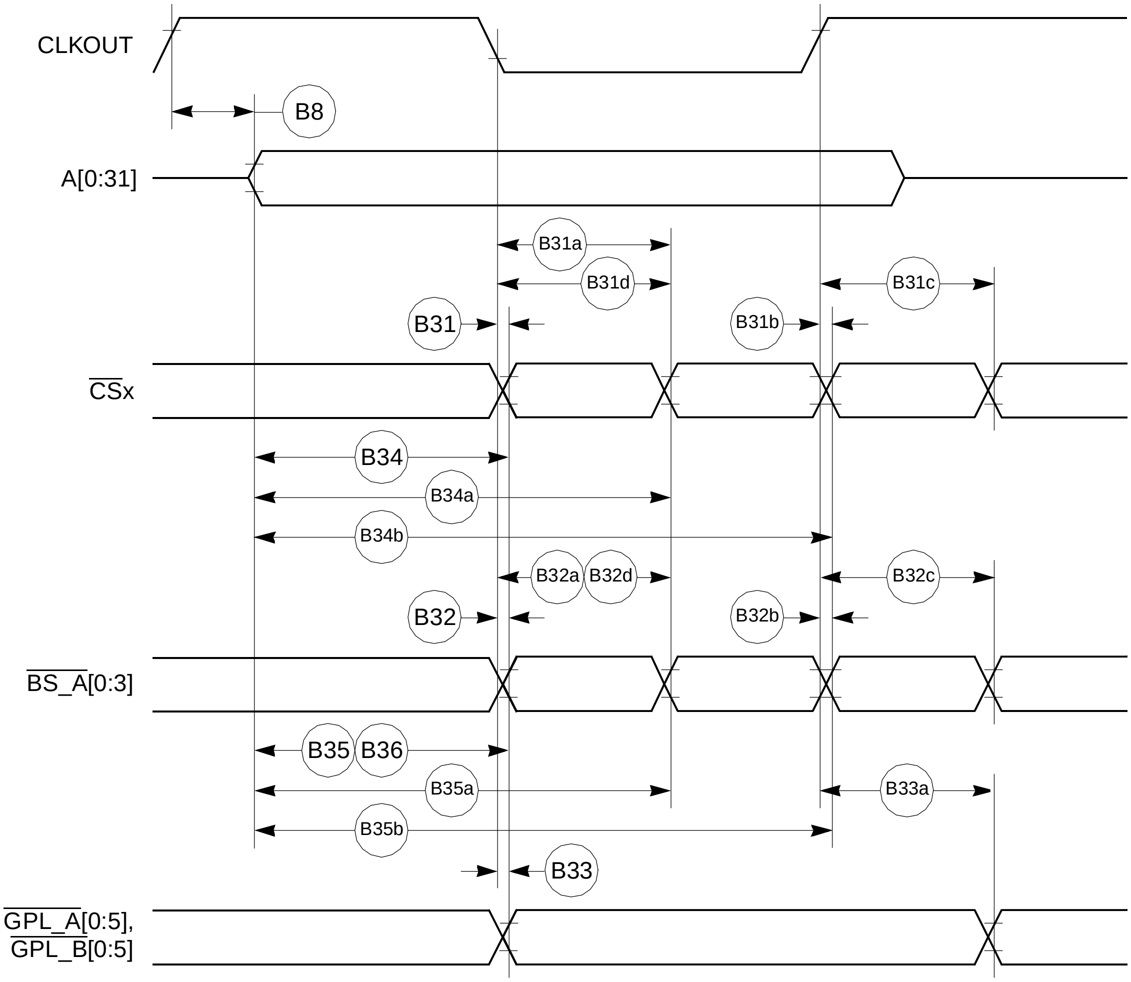


**Figure 19. External Bus Timing (UPM Controlled Signals)**

Figure 20 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

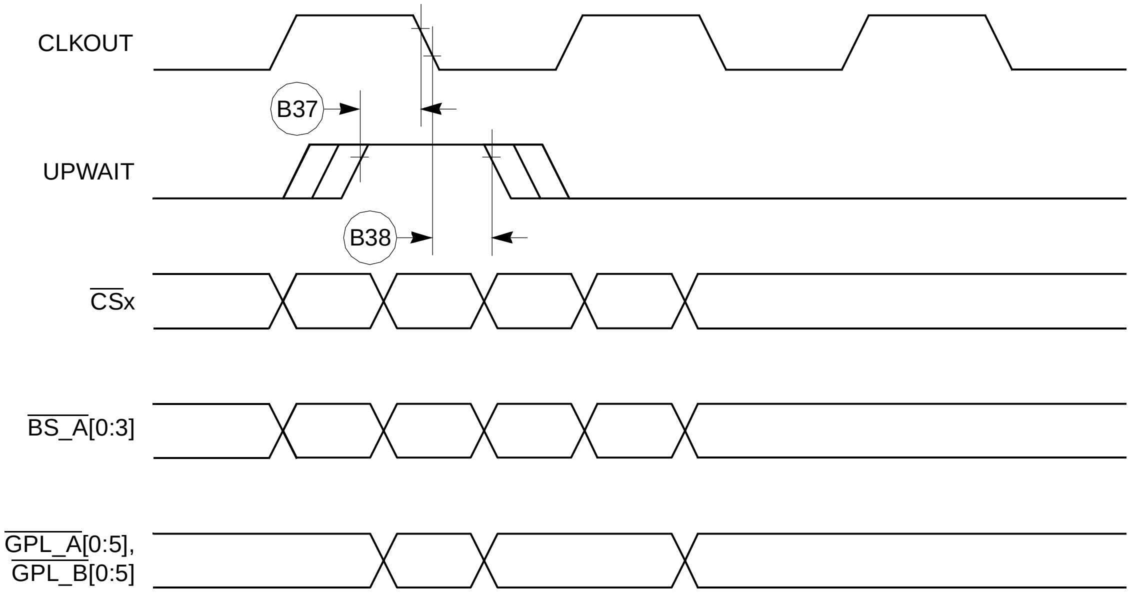


**Figure 20. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing**

Figure 21 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

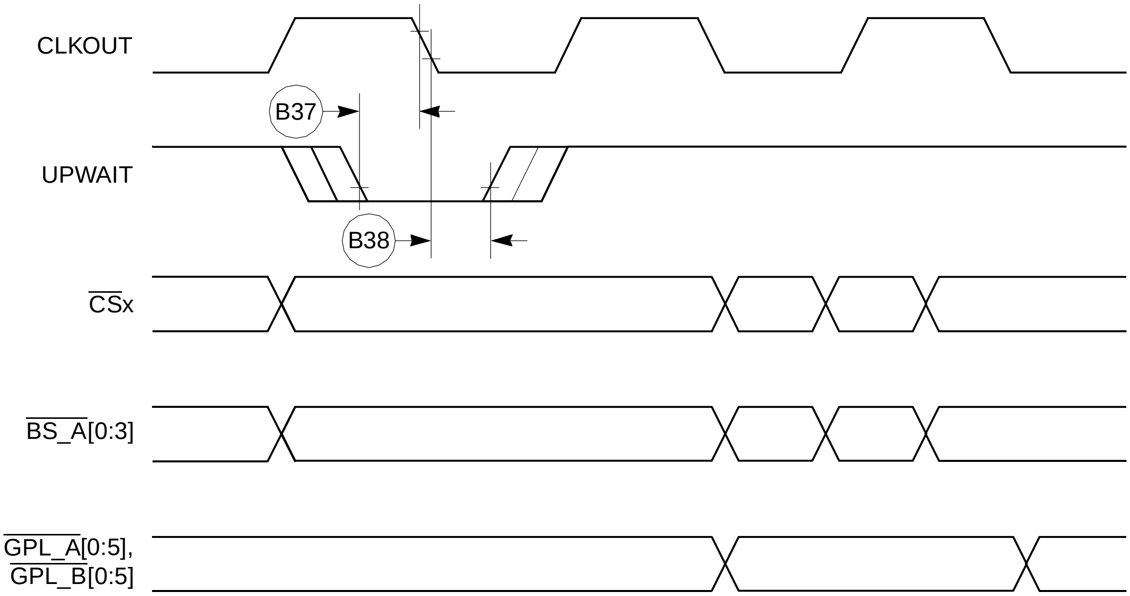


**Figure 21. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing**

Figure 22 provides the timing for the synchronous external master access controlled by the GPCM.

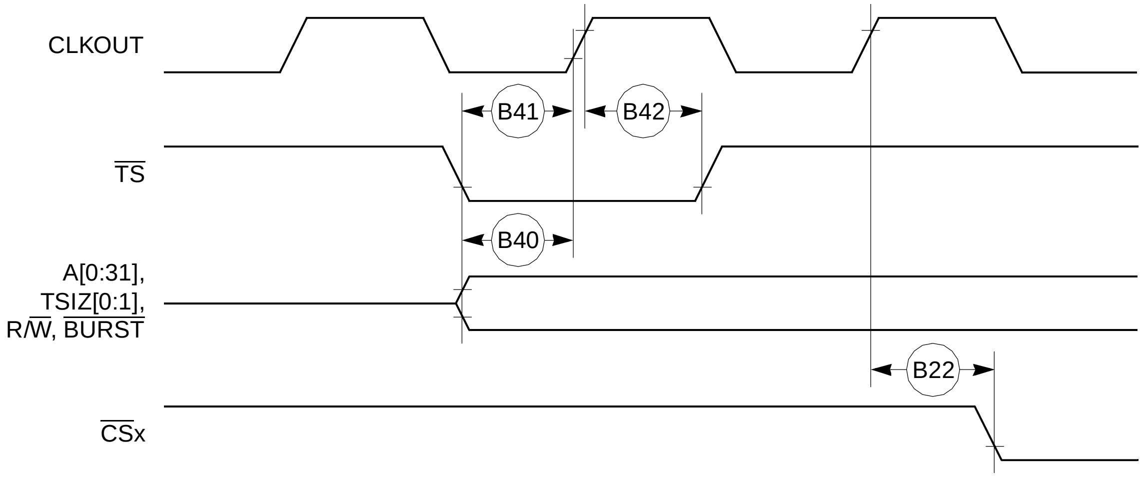


Figure 22. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 23 provides the timing for the asynchronous external master memory access controlled by the GPCM.

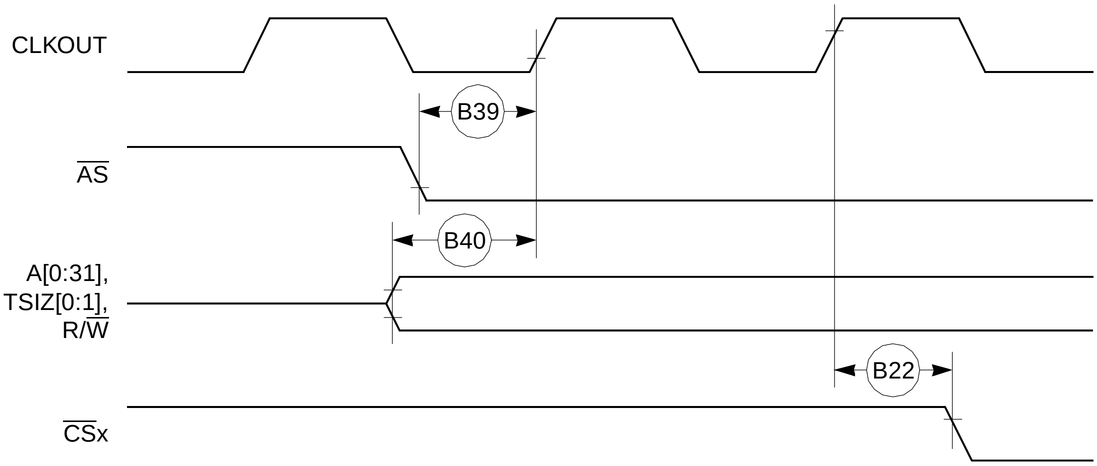


Figure 23. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 24 provides the timing for the asynchronous external master control signals negation.

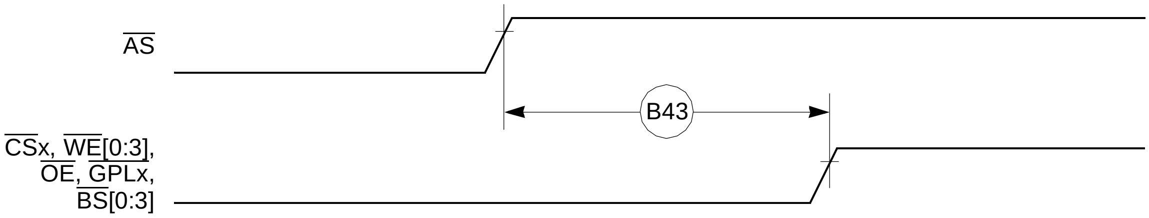


Figure 24. Asynchronous External Master—Control Signals Negation Timing

Table 11 provides the interrupt timing for the MPC875/MPC870.

Table 11. Interrupt Timing

| Num | Characteristic[1] | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| I39 | $\overline{\text{IRQ}}$x valid to CLKOUT rising edge (setup time) | 6.00 | | ns |
| I40 | $\overline{\text{IRQ}}$x hold time after CLKOUT | 2.00 | | ns |
| I41 | $\overline{\text{IRQ}}$x pulse width low | 3.00 | | ns |
| I42 | $\overline{\text{IRQ}}$x pulse width high | 3.00 | | ns |
| I43 | $\overline{\text{IRQ}}$x edge-to-edge time | $4 \times T_{\text{CLOCKOUT}}$ | | — |

[1] The I39 and I40 timings describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT. The I41, I42, and I43 timings are specified to allow correct functioning of the $\overline{\text{IRQ}}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC875/MPC870 is able to support.

Figure 25 provides the interrupt detection timing for the external level-sensitive lines.

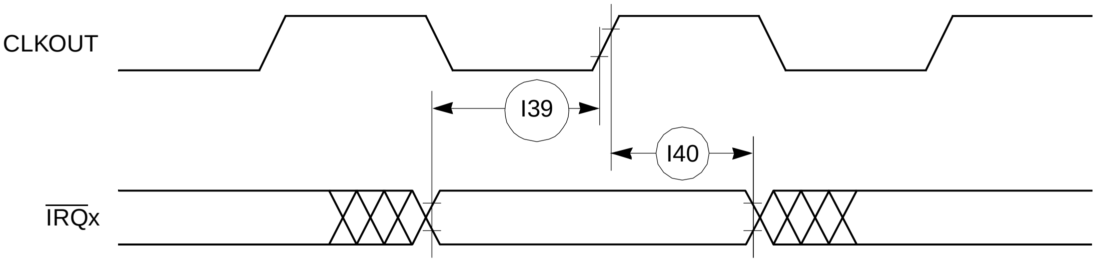


Figure 25. Interrupt Detection Timing for External Level Sensitive Lines

Figure 26 provides the interrupt detection timing for the external edge-sensitive lines.

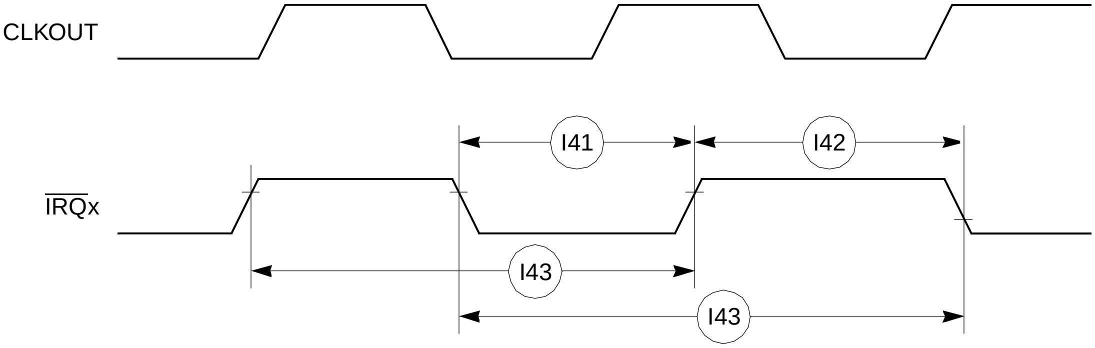


Figure 26. Interrupt Detection Timing for External Edge-Sensitive Lines

Table 12 shows the PCMCIA timing for the MPC875/MPC870.

**Table 12. PCMCIA Timing**

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| P44 | A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted[1] (MIN = 0.75 × B1 – 2.00) | 20.70 | — | 16.70 | — | 9.40 | — | 7.40 | — | ns |
| P45 | A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1] (MIN = 1.00 × B1 – 2.00) | 28.30 | — | 23.00 | — | 13.20 | — | 10.50 | — | ns |
| P46 | CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 × B1 + 8.00) | 7.60 | 15.60 | 6.30 | 14.30 | 3.80 | 11.80 | 3.13 | 11.13 | ns |
| P47 | CLKOUT to $\overline{\text{REG}}$ invalid (MIN = 0.25 × B1 + 1.00) | 8.60 | — | 7.30 | — | 4.80 | — | 4.125 | — | ns |
| P48 | CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = 0.25 × B1 + 8.00) | 7.60 | 15.60 | 6.30 | 14.30 | 3.80 | 11.80 | 3.13 | 11.13 | ns |
| P49 | CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = 0.25 × B1 + 8.00) | 7.60 | 15.60 | 6.30 | 14.30 | 3.80 | 11.80 | 3.13 | 11.13 | ns |
| P50 | CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 × B1 + 11.00) | — | 11.00 | — | 11.00 | — | 11.00 | — | 11.00 | ns |
| P51 | CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 × B1 + 11.00) | 2.00 | 11.00 | 2.00 | 11.00 | 2.00 | 11.00 | 2.00 | 11.00 | ns |
| P52 | CLKOUT to ALE assert time (MAX = 0.25 × B1 + 6.30) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.40 | ns |
| P53 | CLKOUT to ALE negate time (MAX = 0.25 × B1 + 8.00) | — | 15.60 | — | 14.30 | — | 11.80 | — | 11.13 | ns |
| P54 | $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1] (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.125 | — | ns |
| P55 | $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 × B1 + 8.00) | 8.00 | — | 8.00 | — | 8.00 | — | 8.00 | — | ns |
| P56 | CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 × B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |

---

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.
These synchronous timings define when the $\overline{\text{WAITA}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITA}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC885 PowerQUICC™ Family Reference Manual*.

Figure 27 provides the PCMCIA access cycle timing for the external bus read.

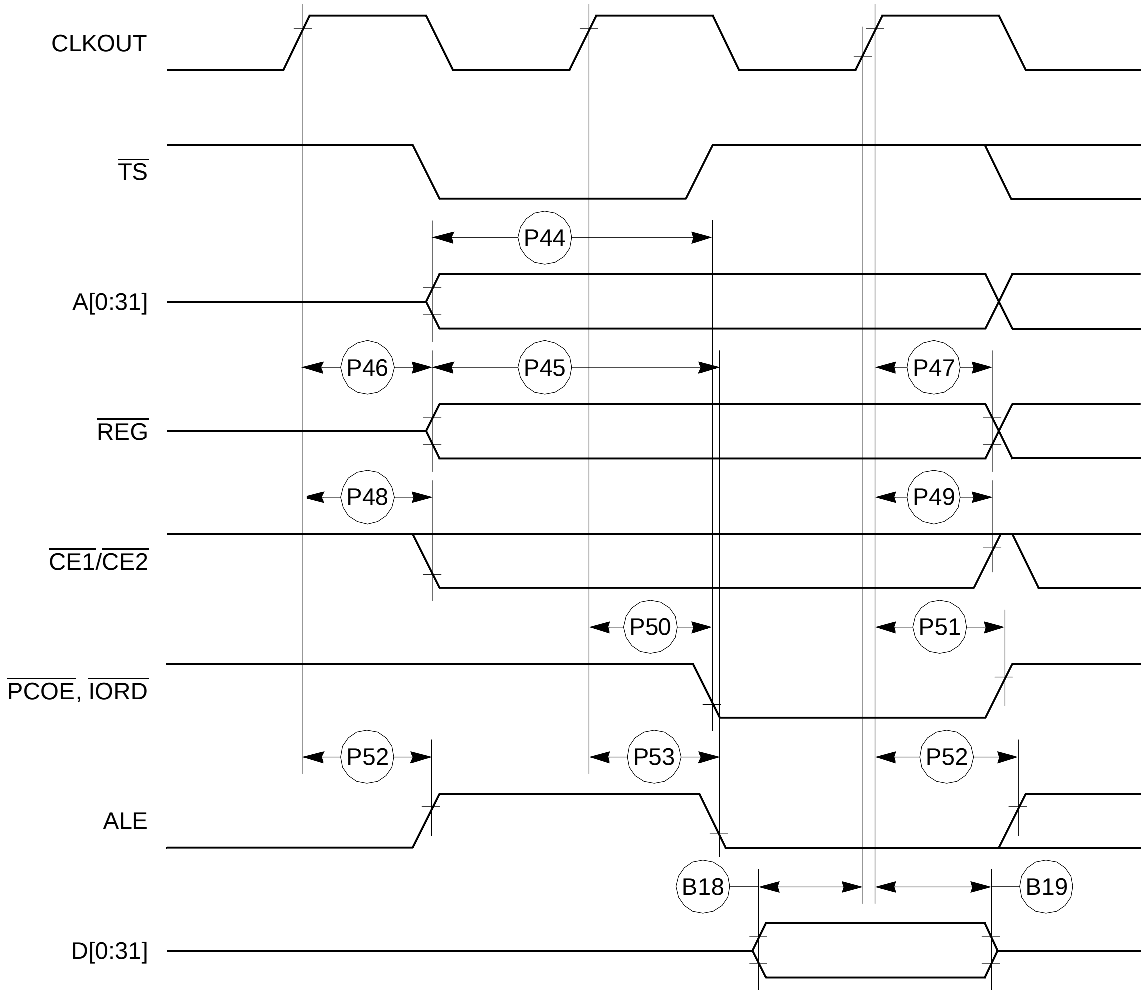


Figure 27. PCMCIA Access Cycles Timing External Bus Read

Figure 28 provides the PCMCIA access cycle timing for the external bus write.

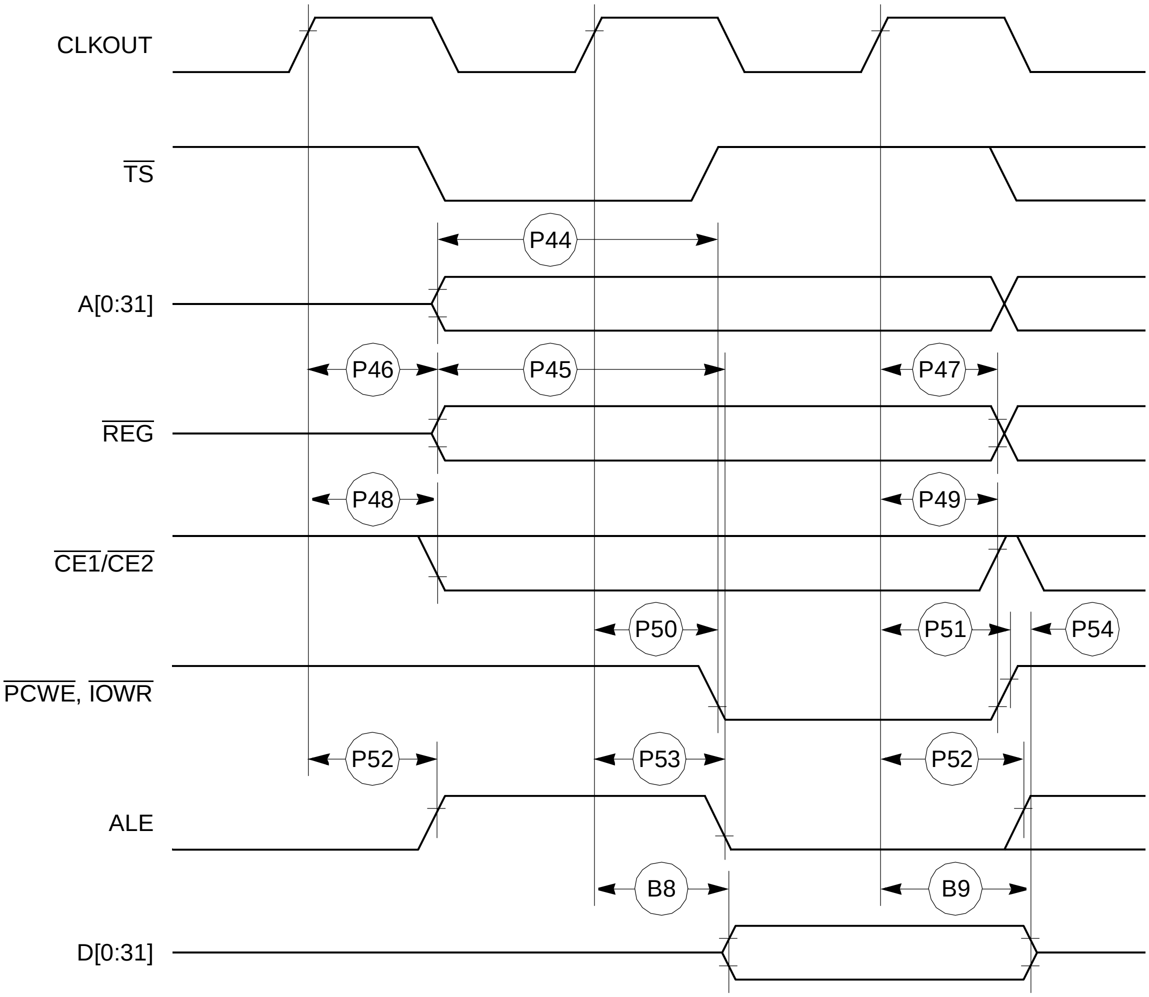


Figure 28. PCMCIA Access Cycles Timing External Bus Write

Figure 29 provides the PCMCIA $\overline{\text{WAIT}}$ signals detection timing.

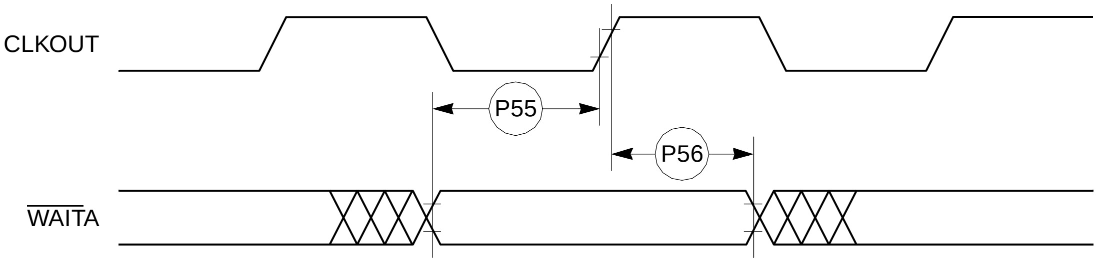


Figure 29. PCMCIA $\overline{\text{WAIT}}$ Signals Detection Timing

Table 13 shows the PCMCIA port timing for the MPC875/MPC870.

**Table 13. PCMCIA Port Timing**

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| P57 | CLKOUT to OPx valid<br>(MAX = 0.00 × B1 + 19.00) | — | 19.00 | — | 19.00 | — | 19.00 | — | 19.00 | ns |
| P58 | $\overline{\text{HRESET}}$ negated to OPx drive[1]<br>(MIN = 0.75 × B1 + 3.00) | 25.70 | — | 21.70 | — | 14.40 | — | 12.40 | — | ns |
| P59 | IP_Xx valid to CLKOUT rising edge<br>(MIN = 0.00 × B1 + 5.00) | 5.00 | — | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| P60 | CLKOUT rising edge to IP_Xx invalid<br>(MIN = 0.00 × B1 + 1.00) | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |

[1] OP2 and OP3 only.

Figure 30 provides the PCMCIA output port timing for the MPC875/MPC870.

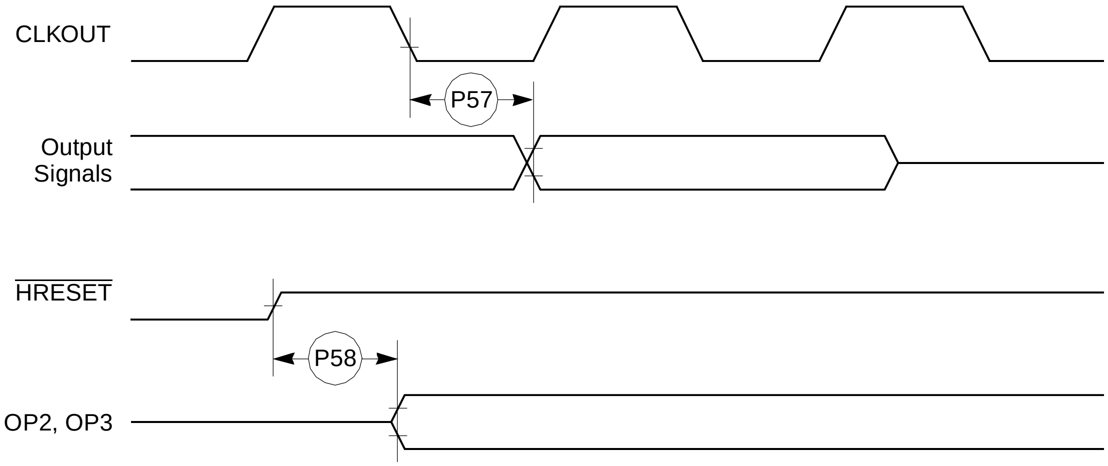


Figure 30. PCMCIA Output Port Timing

Figure 31 provides the PCMCIA input port timing for the MPC875/MPC870.

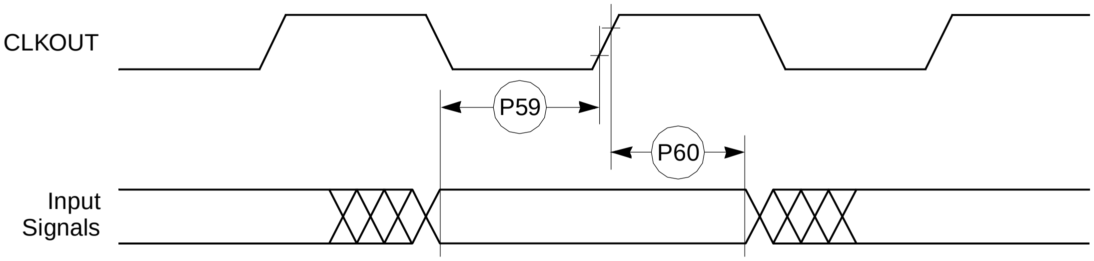


Figure 31. PCMCIA Input Port Timing

Table 14 shows the debug port timing for the MPC875/MPC870.

**Table 14. Debug Port Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| D61 | DSCK cycle time | $3 \times T_{CLOCKOUT}$ | | — |
| D62 | DSCK clock pulse width | $1.25 \times T_{CLOCKOUT}$ | | — |
| D63 | DSCK rise and fall times | 0.00 | 3.00 | ns |
| D64 | DSDI input data setup time | 8.00 | | ns |
| D65 | DSDI data hold time | 5.00 | | ns |
| D66 | DSCK low to DSDO data valid | 0.00 | 15.00 | ns |
| D67 | DSCK low to DSDO invalid | 0.00 | 2.00 | ns |

Figure 32 provides the input timing for the debug port clock.

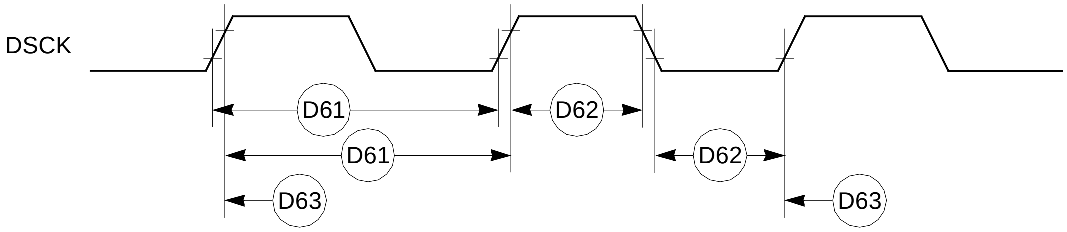


Figure 32. Debug Port Clock Input Timing

Figure 33 provides the timing for the debug port.

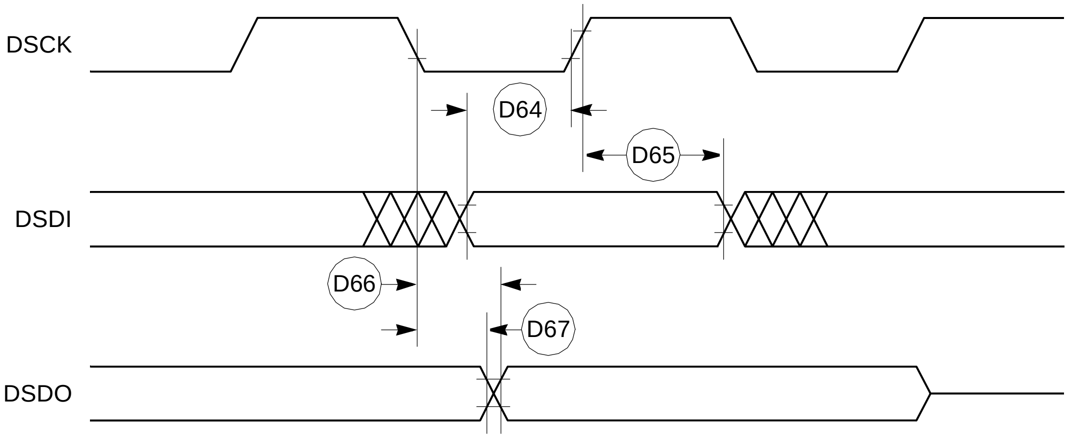


Figure 33. Debug Port Timings

Table 15 shows the reset timing for the MPC875/MPC870.

**Table 15. Reset Timing**

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| R69 | CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00) | — | 20.00 | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| R70 | CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00) | — | 20.00 | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| R71 | $\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1) | 515.20 | — | 425.00 | — | 257.60 | — | 212.50 | — | ns |
| R72 | — | — | — | — | — | — | — | — | — | — |
| R73 | Configuration data to $\overline{\text{HRESET}}$ rising edge setup time (MIN = 15.00 × B1 + 50.00) | 504.50 | — | 425.00 | — | 277.30 | — | 237.50 | — | ns |
| R74 | Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00) | 350.00 | — | 350.00 | — | 350.00 | — | 350.00 | — | ns |
| R75 | Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00) | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R76 | Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00) | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R77 | $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00) | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R78 | $\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 × B1 + 25.00) | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R79 | CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00) | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R80 | DSDI, DSCK setup (MIN = 3.00 × B1) | 90.90 | — | 75.00 | — | 45.50 | — | 37.50 | — | ns |
| R81 | DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00) | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R82 | $\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1) | 242.40 | — | 200.00 | — | 121.20 | — | 100.00 | — | ns |

Figure 34 shows the reset timing for the data bus configuration.

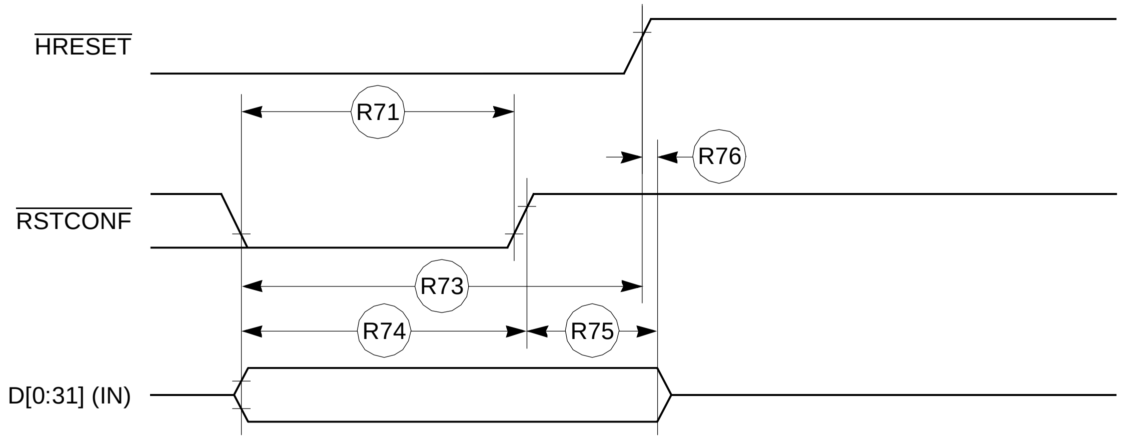


Figure 34. Reset Timing—Configuration from Data Bus

Figure 35 provides the reset timing for the data bus weak drive during configuration.

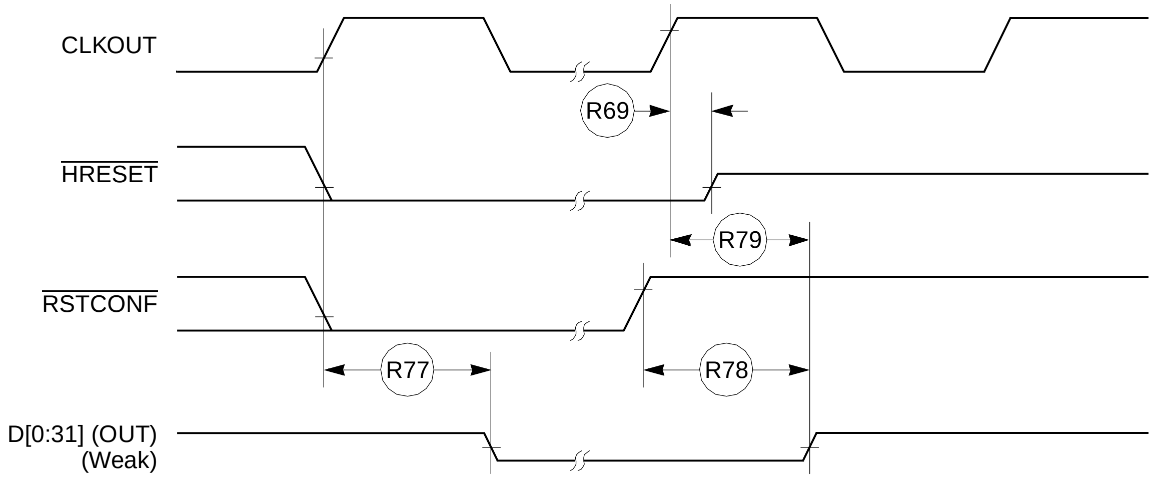


Figure 35. Reset Timing—Data Bus Weak Drive During Configuration

Figure 36 provides the reset timing for the debug port configuration.

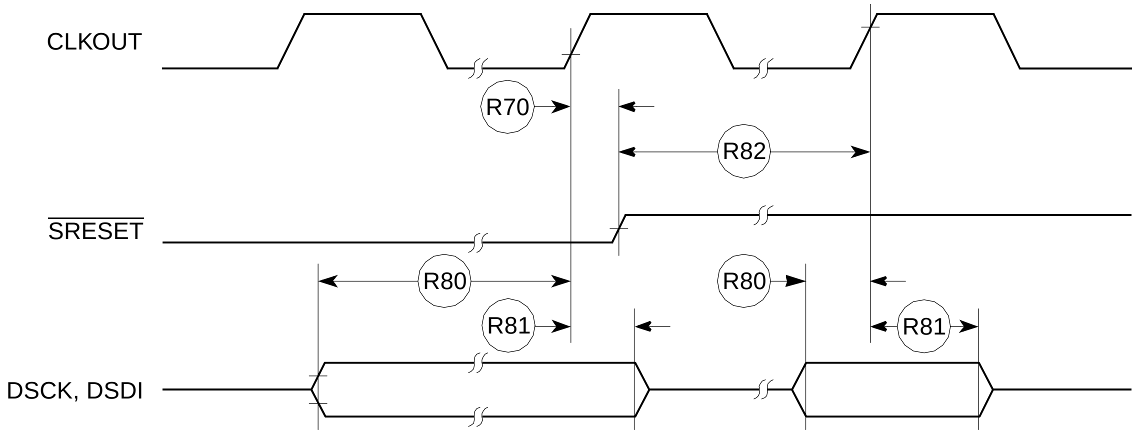


Figure 36. Reset Timing—Debug Port Configuration

# 12 IEEE 1149.1 Electrical Specifications

Table 16 provides the JTAG timings for the MPC875/MPC870 shown in Figure 37 through Figure 40.

**Table 16. JTAG Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| J82 | TCK cycle time | 100.00 | — | ns |
| J83 | TCK clock pulse width measured at 1.5 V | 40.00 | — | ns |
| J84 | TCK rise and fall times | 0.00 | 10.00 | ns |
| J85 | TMS, TDI data setup time | 5.00 | — | ns |
| J86 | TMS, TDI data hold time | 25.00 | — | ns |
| J87 | TCK low to TDO data valid | — | 27.00 | ns |
| J88 | TCK low to TDO data invalid | 0.00 | — | ns |
| J89 | TCK low to TDO high impedance | — | 20.00 | ns |
| J90 | $\overline{\text{TRST}}$ assert time | 100.00 | — | ns |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low | 40.00 | — | ns |
| J92 | TCK falling edge to output valid | — | 50.00 | ns |
| J93 | TCK falling edge to output valid out of high impedance | — | 50.00 | ns |
| J94 | TCK falling edge to output high impedance | — | 50.00 | ns |
| J95 | Boundary scan input valid to TCK rising edge | 50.00 | — | ns |
| J96 | TCK rising edge to boundary scan input invalid | 50.00 | — | ns |

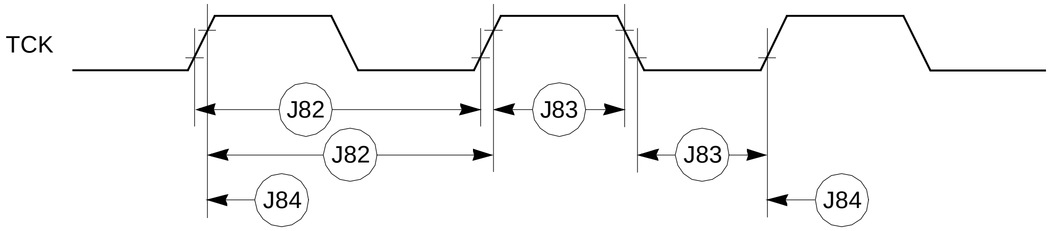


**Figure 37. JTAG Test Clock Input Timing**

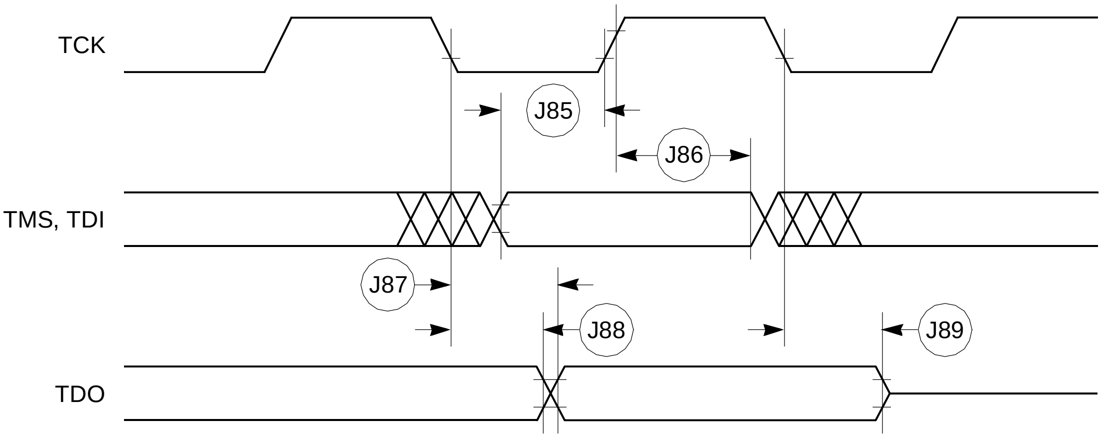


Figure 38. JTAG Test Access Port Timing Diagram

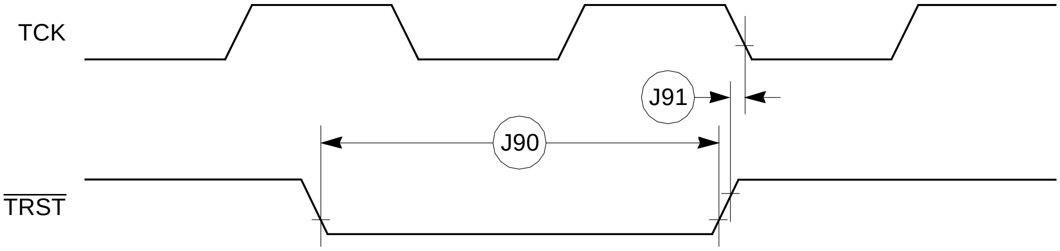


Figure 39. JTAG $\overline{\text{TRST}}$ Timing Diagram

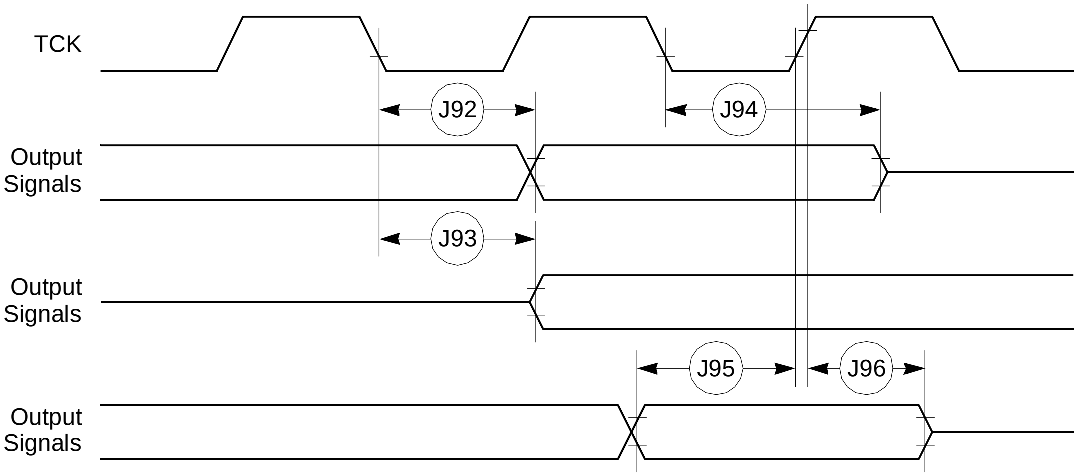


Figure 40. Boundary Scan (JTAG) Timing Diagram

# 13 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC875/MPC870.

## 13.1 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for Port C interrupts.

**Table 17. Port C Interrupt Timing**

| Num | Characteristic | 33.34 MHz | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 35 | Port C interrupt pulse width low (edge-triggered mode) | 55 | — | ns |
| 36 | Port C interrupt minimum time between active edges | 55 | — | ns |

Figure 41 shows the Port C interrupt detection timing.

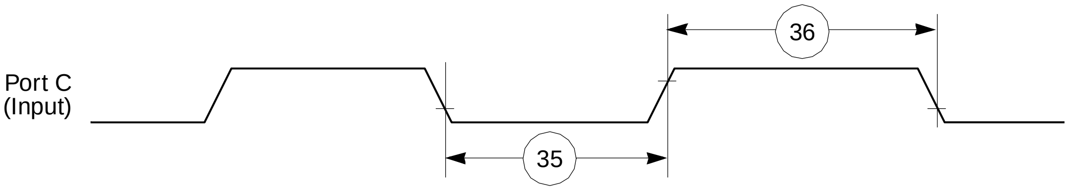


**Figure 41. Port C Interrupt Detection Timing**

## 13.2 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 42 through Figure 45.

**Table 18. IDMA Controller Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 40 | $\overline{\text{DREQ}}$ setup time to clock high | 7 | — | ns |
| 41 | $\overline{\text{DREQ}}$ hold time from clock high[1] | TBD | — | ns |
| 42 | $\overline{\text{SDACK}}$ assertion delay from clock high | — | 12 | ns |
| 43 | $\overline{\text{SDACK}}$ negation delay from clock low | — | 12 | ns |
| 44 | $\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low | — | 20 | ns |
| 45 | $\overline{\text{SDACK}}$ negation delay from clock high | — | 15 | ns |
| 46 | $\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$) | 7 | — | ns |

---

[1] Applies to high-to-low mode (EDM = 1).

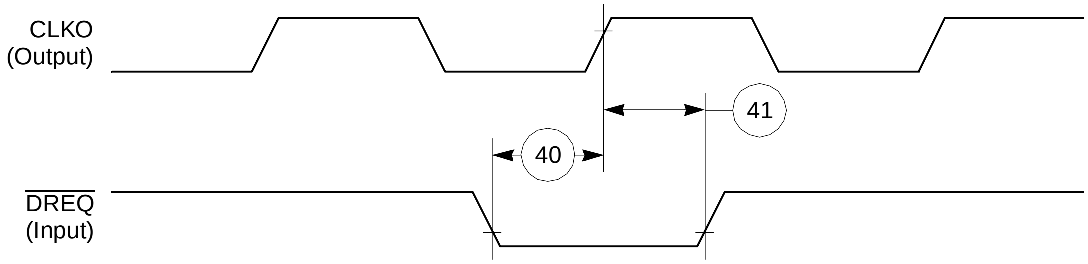


Figure 42. IDMA External Requests Timing Diagram

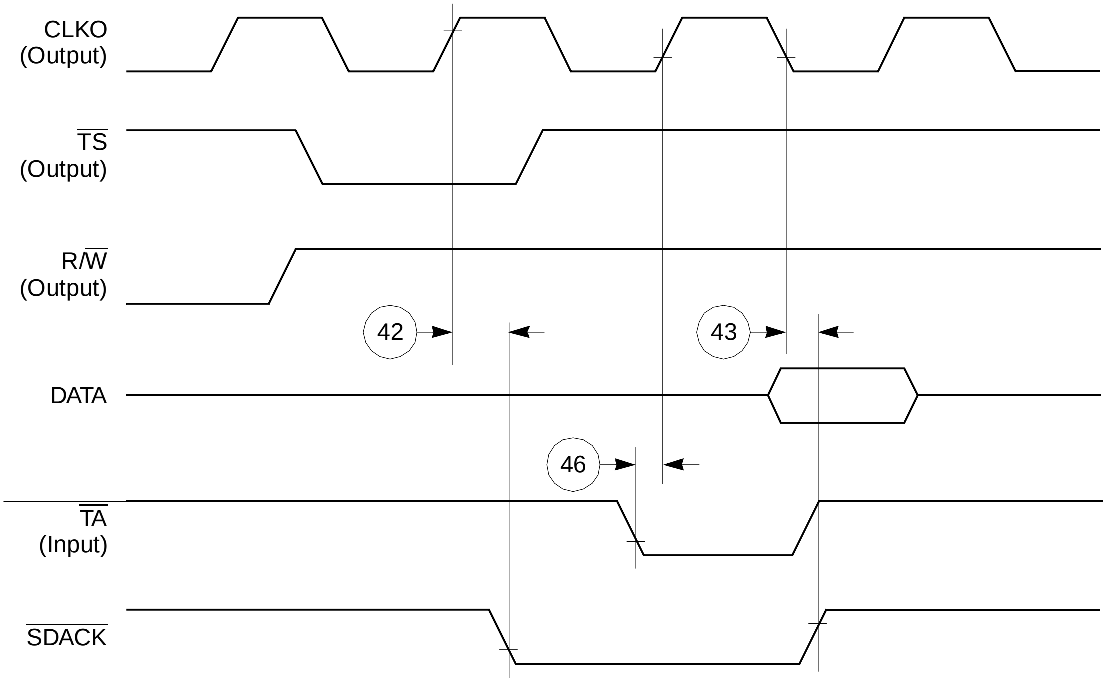


Figure 43. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

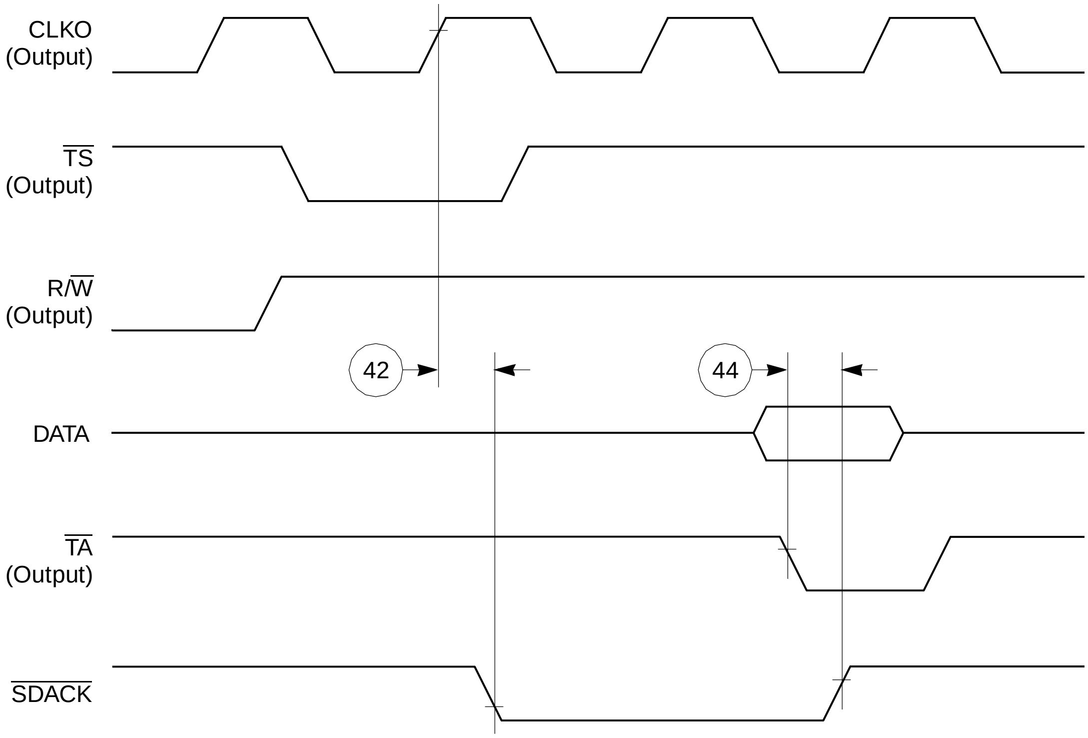


Figure 44. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

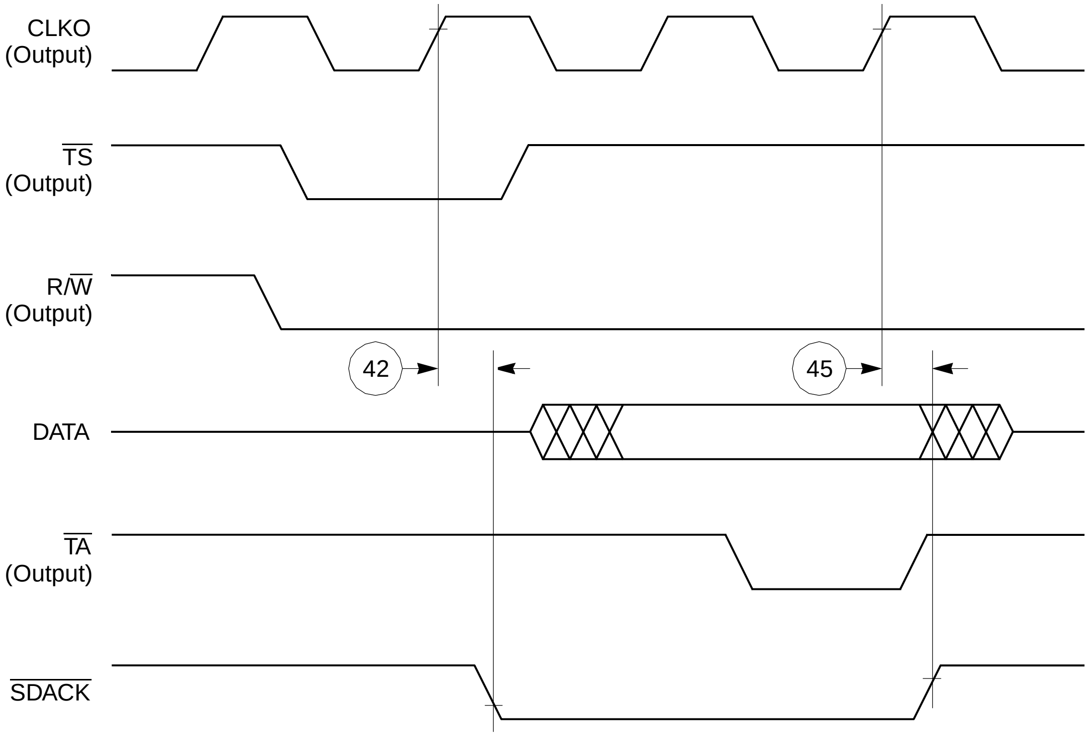


Figure 45. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

## 13.3 Baud Rate Generator AC Electrical Specifications

Table 19 provides the baud rate generator timings as shown in Figure 46.

**Table 19. Baud Rate Generator Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 50 | BRGO rise and fall time | — | 10 | ns |
| 51 | BRGO duty cycle | 40 | 60 | % |
| 52 | BRGO cycle | 40 | — | ns |

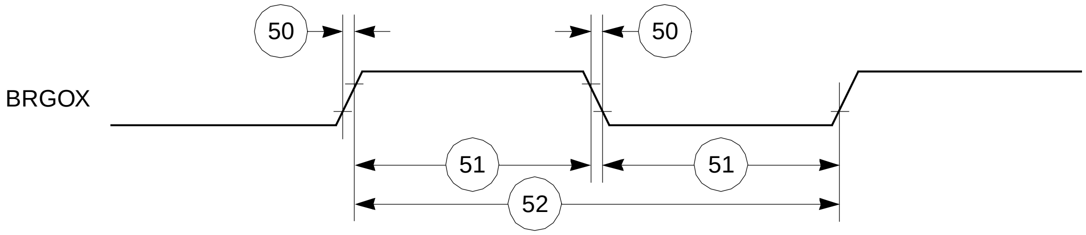


**Figure 46. Baud Rate Generator Timing Diagram**

## 13.4 Timer AC Electrical Specifications

Table 20 provides the general-purpose timer timings as shown in Figure 47.

**Table 20. Timer Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 61 | TIN/$\overline{\text{TGATE}}$ rise and fall time | 10 | — | ns |
| 62 | TIN/$\overline{\text{TGATE}}$ low time | 1 | — | clk |
| 63 | TIN/$\overline{\text{TGATE}}$ high time | 2 | — | clk |
| 64 | TIN/$\overline{\text{TGATE}}$ cycle time | 3 | — | clk |
| 65 | CLKO low to $\overline{\text{TOUT}}$ valid | 3 | 25 | ns |

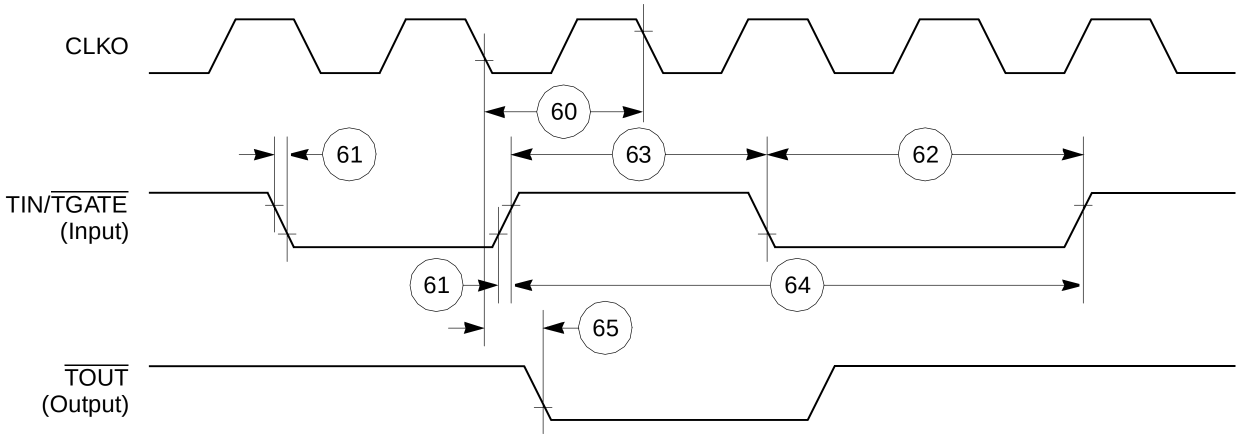


**Figure 47. CPM General-Purpose Timers Timing Diagram**

## 13.5 Serial Interface AC Electrical Specifications

Table 21 provides the serial interface (SI) timings as shown in Figure 48 through Figure 52.

**Table 21. SI Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 70 | L1RCLKB, L1TCLKB frequency (DSC = 0)[1, 2] | — | SYNCCLK/2.5 | MHz |
| 71 | L1RCLKB, L1TCLKB width low (DSC = 0)[2] | P + 10 | — | ns |
| 71a | L1RCLKB, L1TCLKB width high (DSC = 0)[3] | P + 10 | — | ns |
| 72 | L1TXDB, L1ST1 and L1ST2, $\overline{\text{L1RQ}}$, L1CLKO rise/fall time | — | 15.00 | ns |
| 73 | L1RSYNCB, L1TSYNCB valid to L1CLKB edge (SYNC setup time) | 20.00 | — | ns |
| 74 | L1CLKB edge to L1RSYNCB, L1TSYNCB, invalid (SYNC hold time) | 35.00 | — | ns |
| 75 | L1RSYNCB, L1TSYNCB rise/fall time | — | 15.00 | ns |
| 76 | L1RXDB valid to L1CLKB edge (L1RXDB setup time) | 17.00 | — | ns |
| 77 | L1CLKB edge to L1RXDB invalid (L1RXDB hold time) | 13.00 | — | ns |
| 78 | L1CLKB edge to L1ST1 and L1ST2 valid[4] | 10.00 | 45.00 | ns |
| 78A | L1SYNCB valid to L1ST1 and L1ST2 valid | 10.00 | 45.00 | ns |
| 79 | L1CLKB edge to L1ST1 and L1ST2 invalid | 10.00 | 45.00 | ns |
| 80 | L1CLKB edge to L1TXDB valid | 10.00 | 55.00 | ns |
| 80A | L1TSYNCB valid to L1TXDB valid[4] | 10.00 | 55.00 | ns |
| 81 | L1CLKB edge to L1TXDB high impedance | 0.00 | 42.00 | ns |
| 82 | L1RCLKB, L1TCLKB frequency (DSC = 1) | — | 16.00 or SYNCCLK/2 | MHz |
| 83 | L1RCLKB, L1TCLKB width low (DSC = 1) | P + 10 | — | ns |

**Table 21. SI Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 83a | L1RCLKB, L1TCLKB width high (DSC = 1)[3] | P + 10 | — | ns |
| 84 | L1CLKB edge to L1CLKOB valid (DSC = 1) | — | 30.00 | ns |
| 85 | $\overline{\text{L1RQB}}$ valid before falling edge of L1TSYNCB[4] | 1.00 | — | L1TCLK |
| 86 | L1GRB setup time[2] | 42.00 | — | ns |
| 87 | L1GRB hold time | 42.00 | — | ns |
| 88 | L1CLKB edge to L1SYNCB valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0) | — | 0.00 | ns |

[1] The ratio SYNCCLK/L1RCLKB must be greater than 2.5/1.

[2] These specs are valid for IDL mode only.

[3] Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.

[4] These strobes and TxD on the first bit of the frame become valid after the L1CLKB edge or L1SYNCB, whichever comes later.

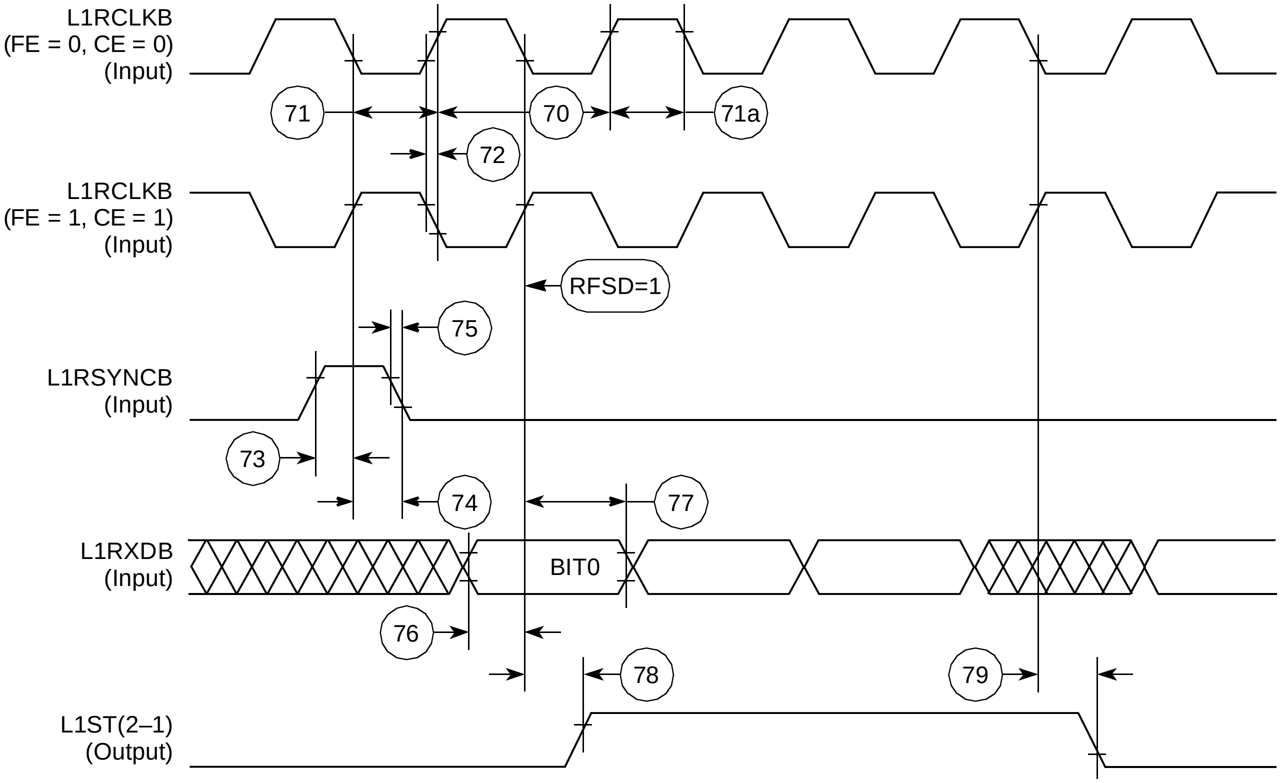


Figure 48. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

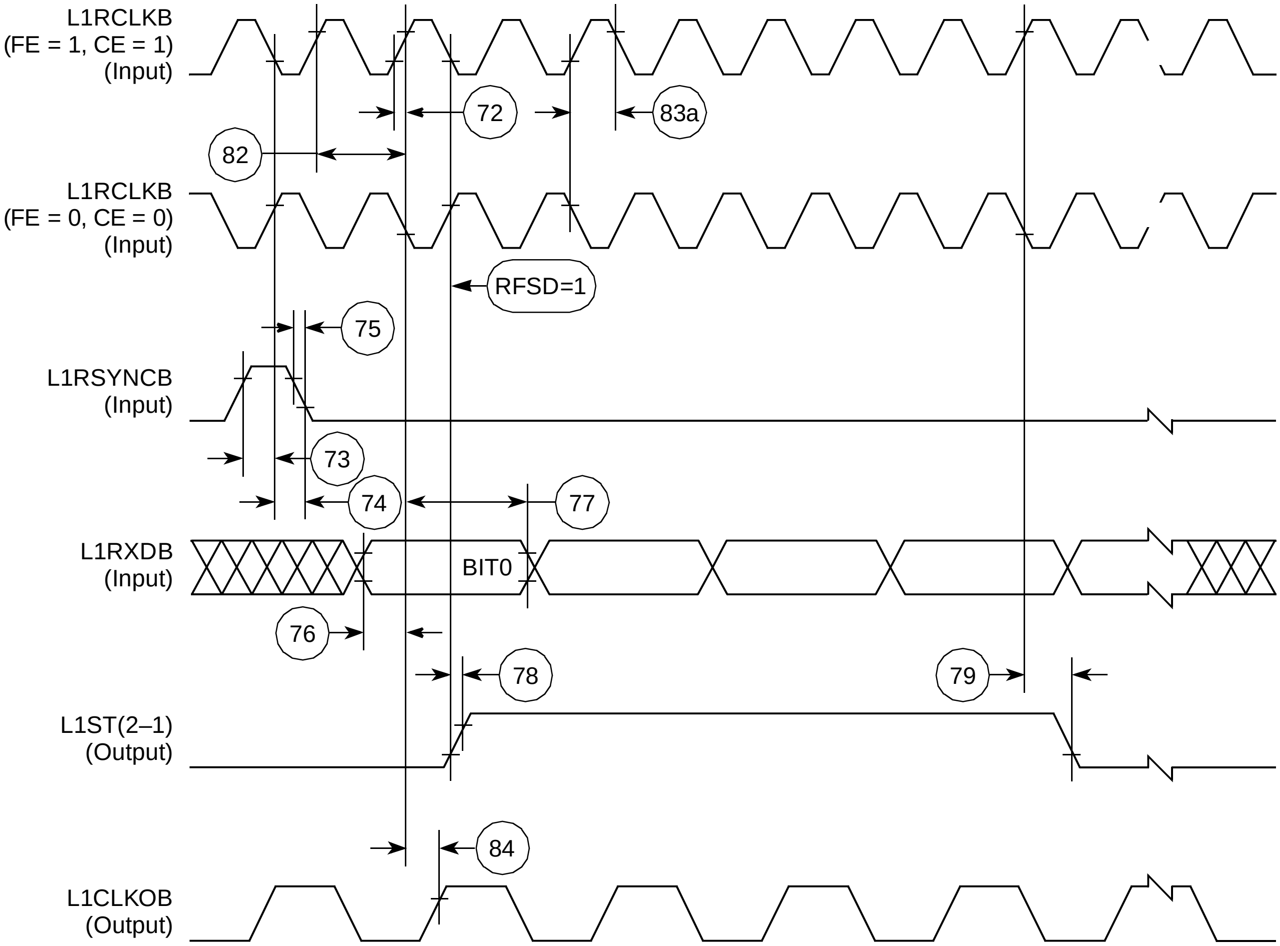


Figure 49. SI Receive Timing with Double-Speed Clocking (DSC = 1)

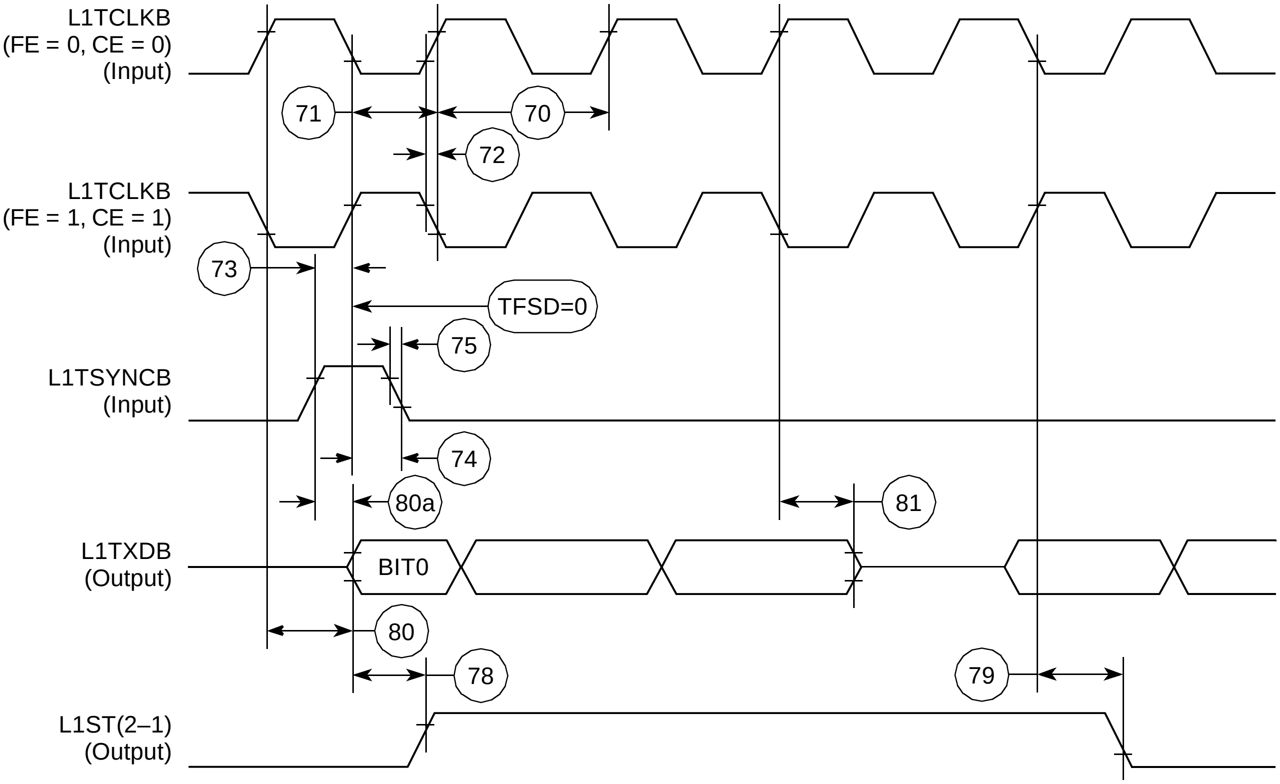


**Figure 50. SI Transmit Timing Diagram (DSC = 0)**

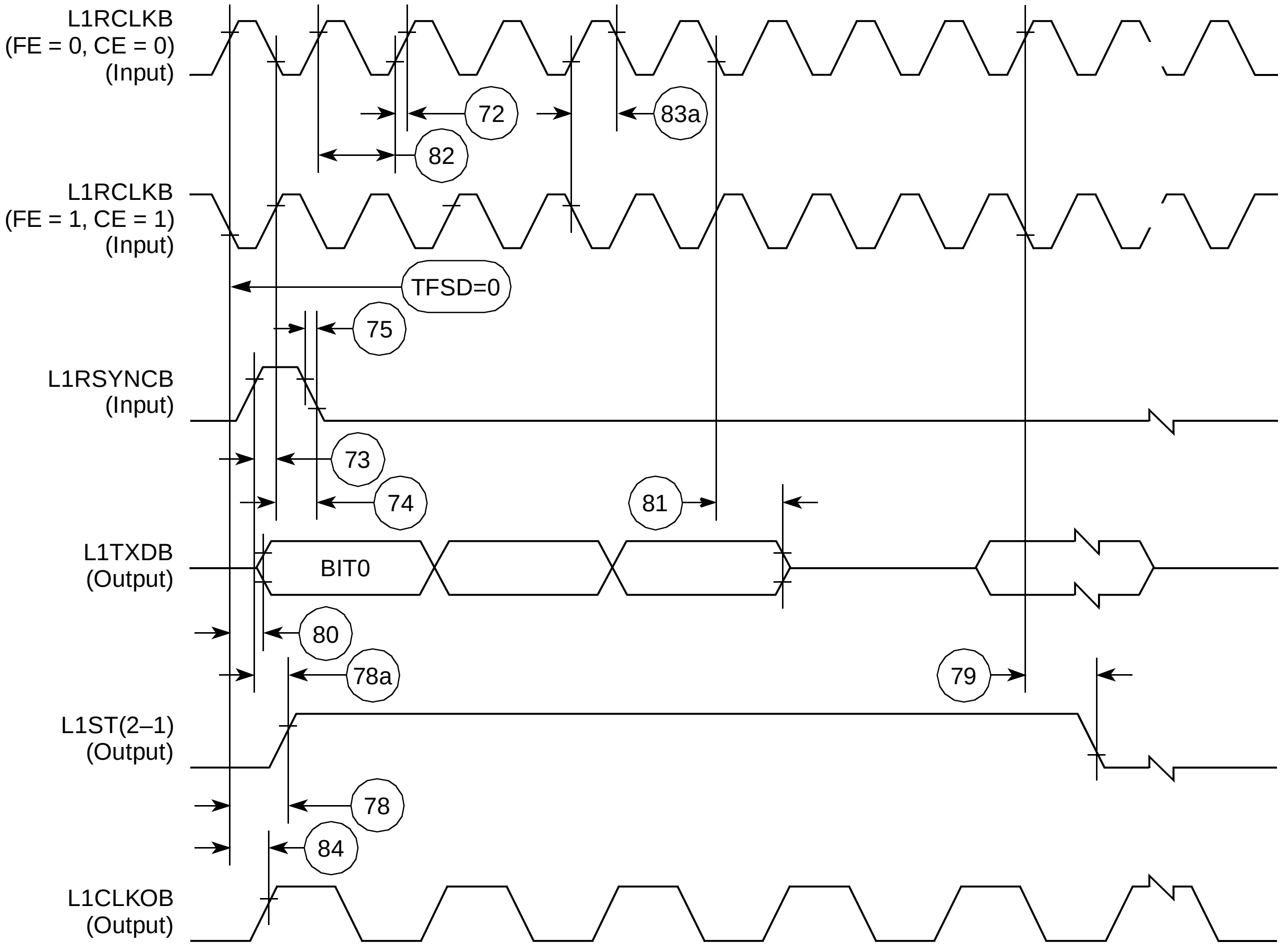


Figure 51. SI Transmit Timing with Double Speed Clocking (DSC = 1)

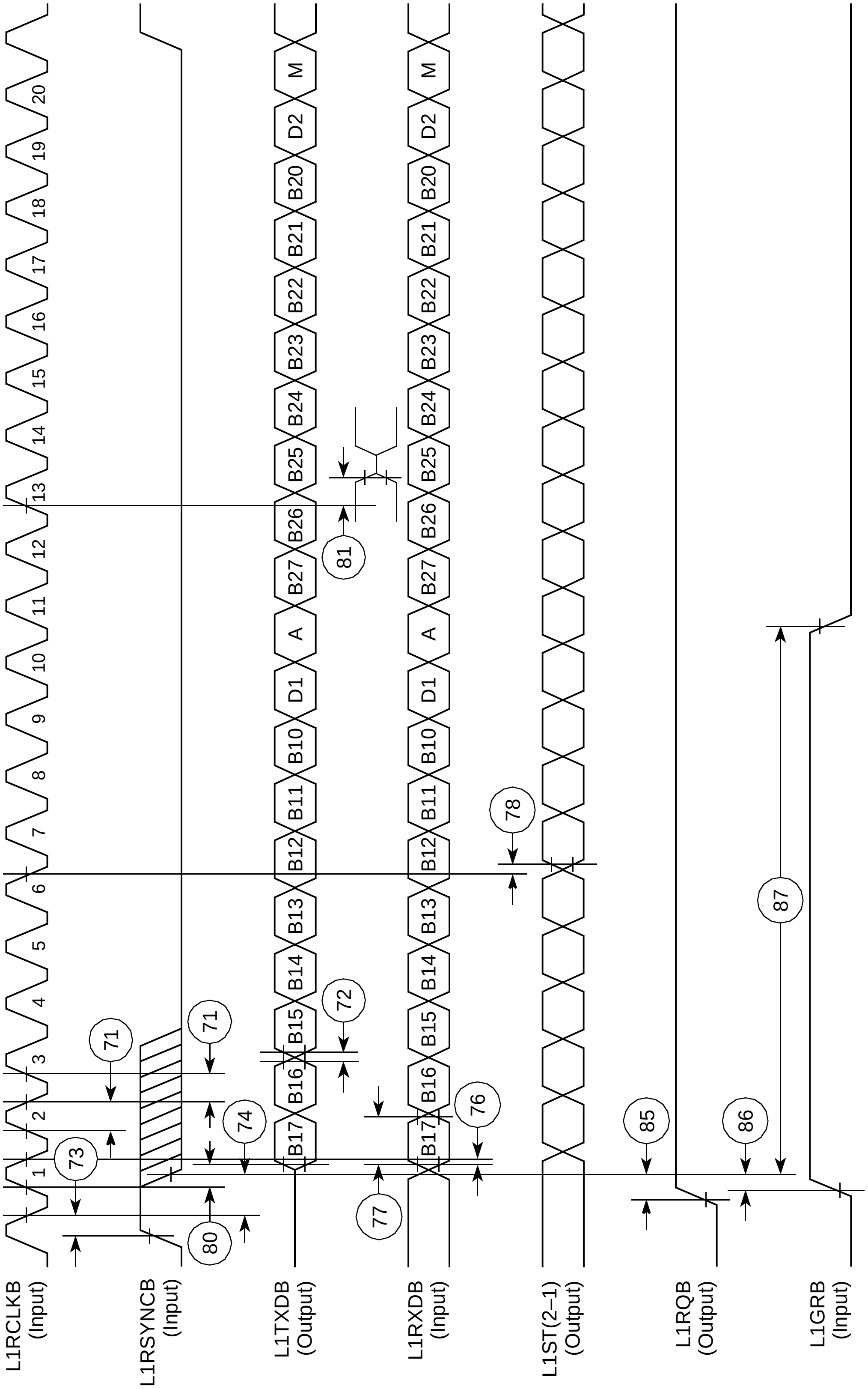


Figure 52. IDL Timing

## 13.6 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

**Table 22. NMSI External Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK3 and TCLK3 width high[1] | 1/SYNCCLK | — | ns |
| 101 | RCLK3 and TCLK3 width low | 1/SYNCCLK + 5 | — | ns |
| 102 | RCLK3 and TCLK3 rise/fall time | — | 15.00 | ns |
| 103 | TXD3 active delay (from TCLK3 falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{\mathrm{RTS3}}$ active/inactive delay (from TCLK3 falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{\mathrm{CTS3}}$ setup time to TCLK3 rising edge | 5.00 | — | ns |
| 106 | RXD3 setup time to RCLK3 rising edge | 5.00 | — | ns |
| 107 | RXD3 hold time from RCLK3 rising edge[2] | 5.00 | — | ns |
| 108 | $\overline{\mathrm{CD3}}$ setup time to RCLK3 rising edge | 5.00 | — | ns |

[1] The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater than or equal to 2.25/1.

[2] Also applies to $\overline{\mathrm{CD}}$ and $\overline{\mathrm{CTS}}$ hold time when they are used as external SYNC signals.

Table 23 provides the NMSI internal clock timing.

**Table 23. NMSI Internal Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK3 and TCLK3 frequency[1] | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLK3 and TCLK3 rise/fall time | — | — | ns |
| 103 | TXD3 active delay (from TCLK3 falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{\mathrm{RTS3}}$ active/inactive delay (from TCLK3 falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{\mathrm{CTS3}}$ setup time to TCLK3 rising edge | 40.00 | — | ns |
| 106 | RXD3 setup time to RCLK3 rising edge | 40.00 | — | ns |
| 107 | RXD3 hold time from RCLK3 rising edge[2] | 0.00 | — | ns |
| 108 | $\overline{\mathrm{CD3}}$ setup time to RCLK3 rising edge | 40.00 | — | ns |

[1] The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater or equal to 3/1.

[2] Also applies to $\overline{\mathrm{CD}}$ and $\overline{\mathrm{CTS}}$ hold time when they are used as external SYNC signals.

Figure 53 through Figure 55 show the NMSI timings.

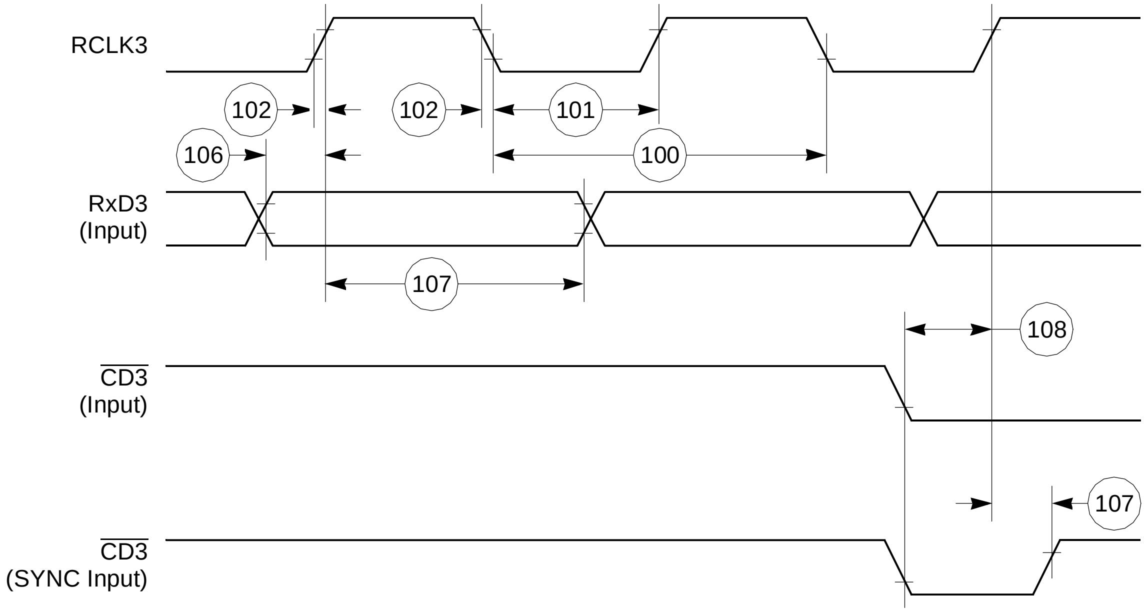


Figure 53. SCC NMSI Receive Timing Diagram

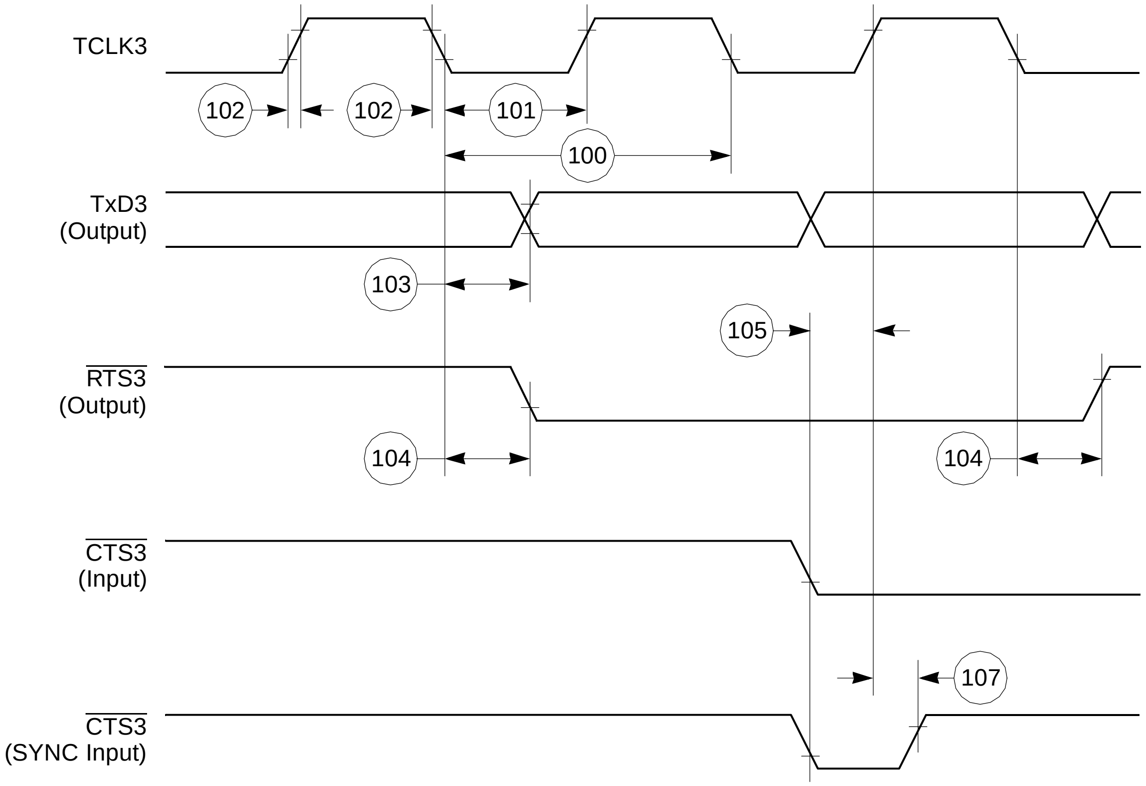


Figure 54. SCC NMSI Transmit Timing Diagram

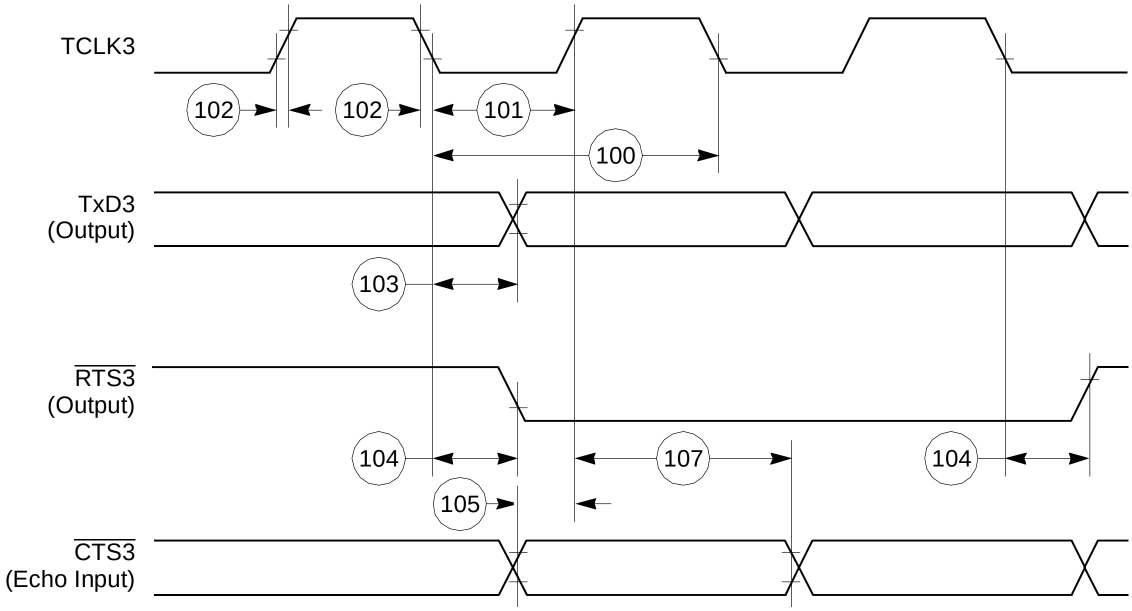


**Figure 55. HDLC Bus Timing Diagram**

## 13.7 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 56 through Figure 58.

**Table 24. Ethernet Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 120 | CLSN width high | 40 | — | ns |
| 121 | RCLK3 rise/fall time | — | 15 | ns |
| 122 | RCLK3 width low | 40 | — | ns |
| 123 | RCLK3 clock period[1] | 80 | 120 | ns |
| 124 | RXD3 setup time | 20 | — | ns |
| 125 | RXD3 hold time | 5 | — | ns |
| 126 | RENA active delay (from RCLK3 rising edge of the last data bit) | 10 | — | ns |
| 127 | RENA width low | 100 | — | ns |
| 128 | TCLK3 rise/fall time | — | 15 | ns |
| 129 | TCLK3 width low | 40 | — | ns |
| 130 | TCLK3 clock period[1] | 99 | 101 | ns |
| 131 | TXD3 active delay (from TCLK3 rising edge) | — | 50 | ns |
| 132 | TXD3 inactive delay (from TCLK3 rising edge) | 6.5 | 50 | ns |
| 133 | TENA active delay (from TCLK3 rising edge) | 10 | 50 | ns |
| 134 | TENA inactive delay (from TCLK3 rising edge) | 10 | 50 | ns |

### Table 24. Ethernet Timing (continued)

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 138 | CLKO1 low to $\overline{\text{SDACK}}$ asserted[2] | — | 20 | ns |
| 139 | CLKO1 low to $\overline{\text{SDACK}}$ negated[2] | — | 20 | ns |

---

[1] The ratios SYNCCLK/RCLK3 and SYNCCLK/TCLK3 must be greater than or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

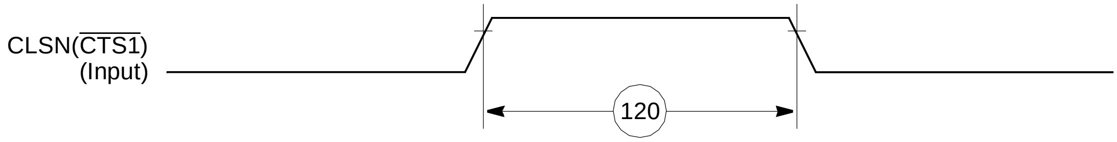


Figure 56. Ethernet Collision Timing Diagram

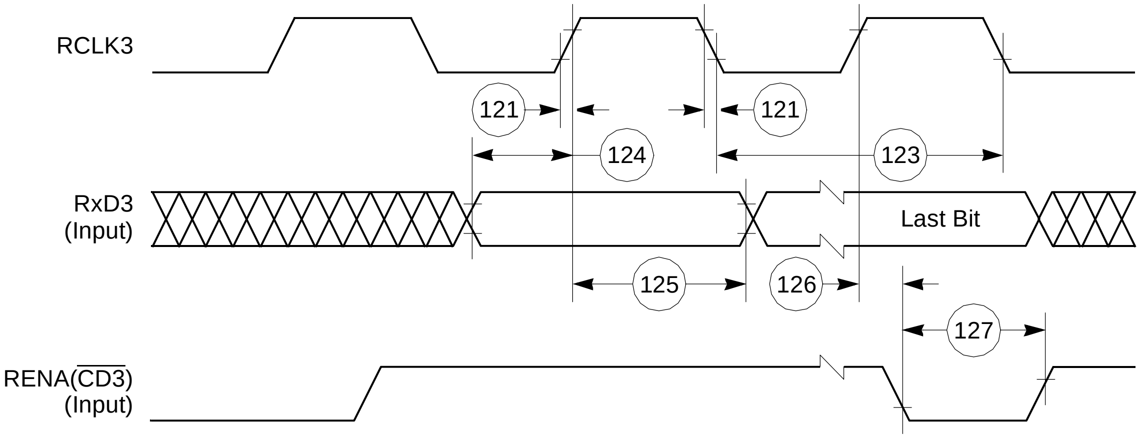
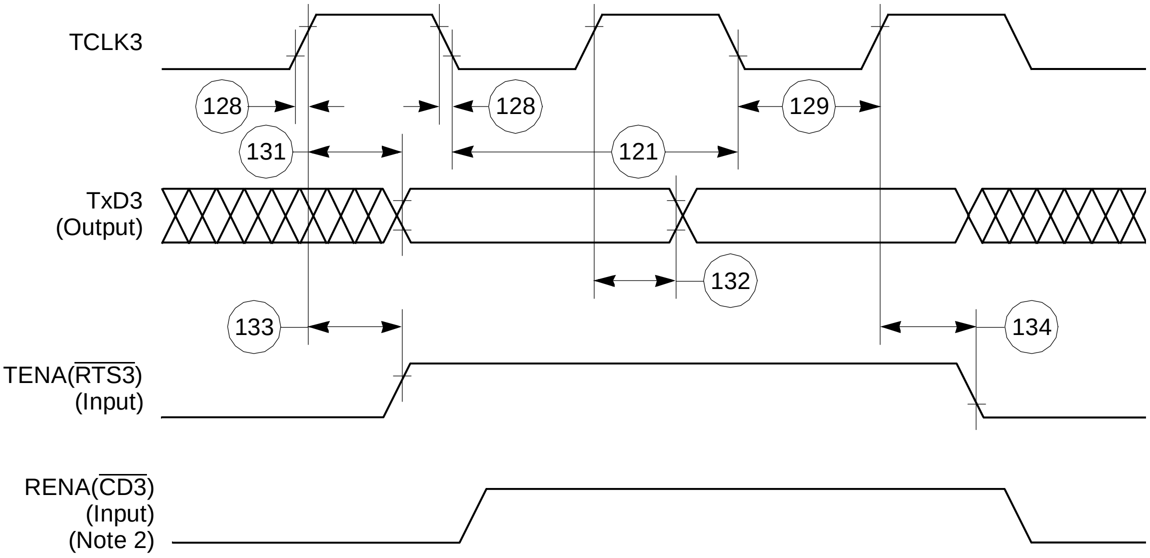


Figure 57. Ethernet Receive Timing Diagram



**Notes:**

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

**Figure 58. Ethernet Transmit Timing Diagram**

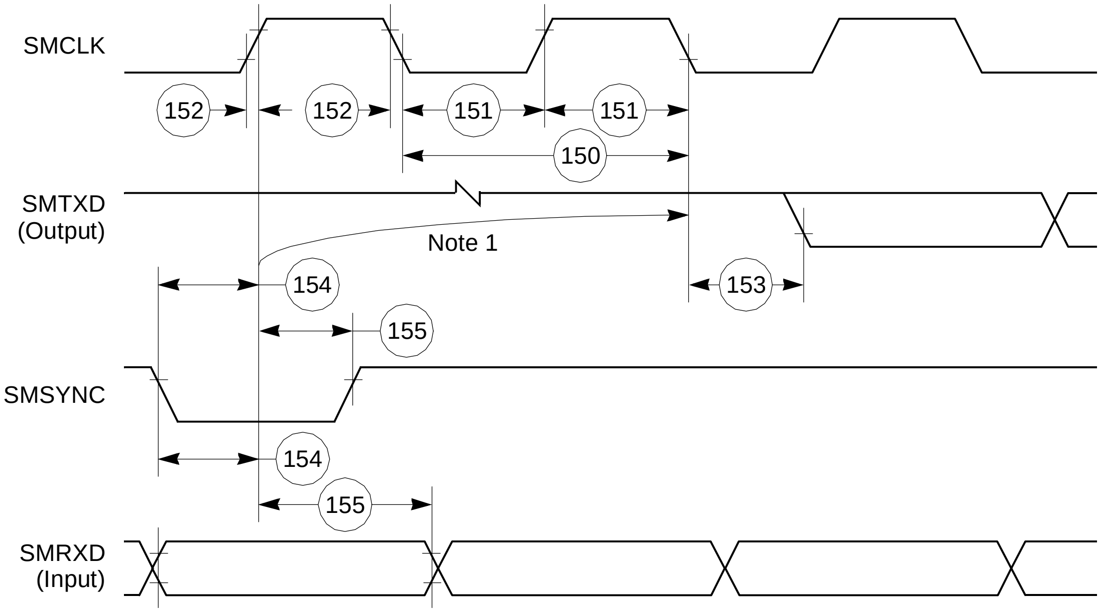
## 13.8 SMC Transparent AC Electrical Specifications

Table 25 provides the SMC transparent timings as shown in Figure 59.

**Table 25. SMC Transparent Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 150 | SMCLK clock period[1] | 100 | — | ns |
| 151 | SMCLK width low | 50 | — | ns |
| 151A | SMCLK width high | 50 | — | ns |
| 152 | SMCLK rise/fall time | — | 15 | ns |
| 153 | SMTXD active delay (from SMCLK falling edge) | 10 | 50 | ns |
| 154 | SMRXD/SMSYNC setup time | 20 | — | ns |
| 155 | RXD1/SMSYNC hold time | 5 | — | ns |

[1] SYNCCLK must be at least twice as fast as SMCLK.



**Note:**
1. This delay is equal to an integer number of character-length clocks.

Figure 59. SMC Transparent Timing Diagram

## 13.9 SPI Master AC Electrical Specifications

Table 26 provides the SPI master timings as shown in Figure 60 and Figure 61.

Table 26. SPI Master Timing

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 160 | Master cycle time | 4 | 1024 | $t_{cyc}$ |
| 161 | Master clock (SCK) high or low time | 2 | 512 | $t_{cyc}$ |
| 162 | Master data setup time (inputs) | 15 | — | ns |
| 163 | Master data hold time (inputs) | 0 | — | ns |
| 164 | Master data valid (after SCK edge) | — | 10 | ns |
| 165 | Master data hold time (outputs) | 0 | — | ns |
| 166 | Rise time output | — | 15 | ns |
| 167 | Fall time output | — | 15 | ns |

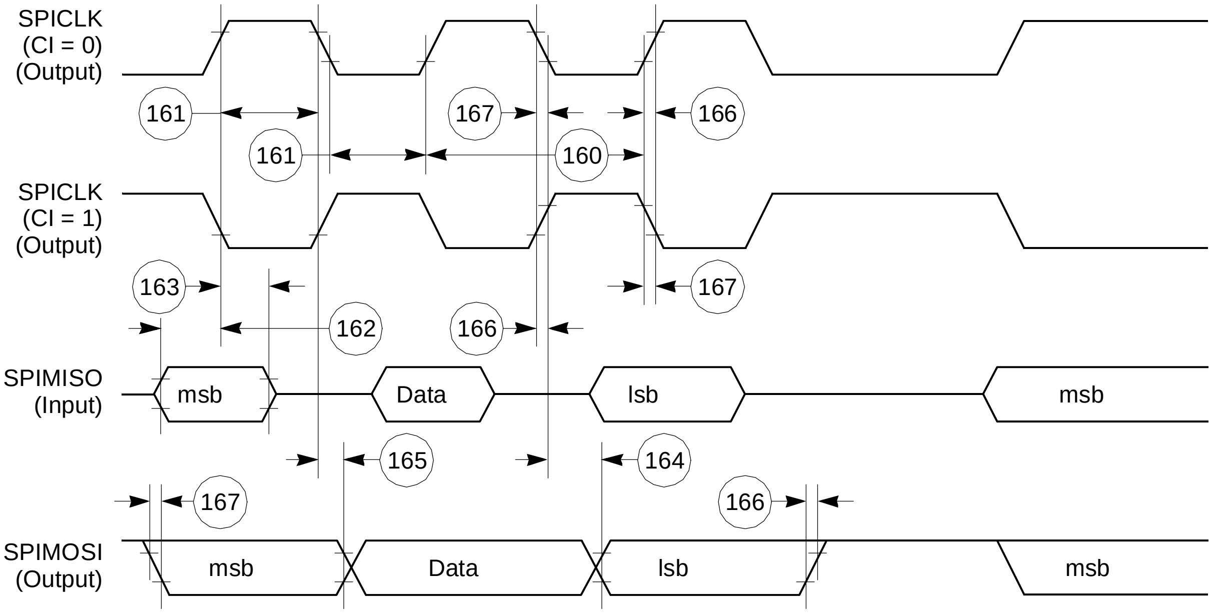


Figure 60. SPI Master (CP = 0) Timing Diagram

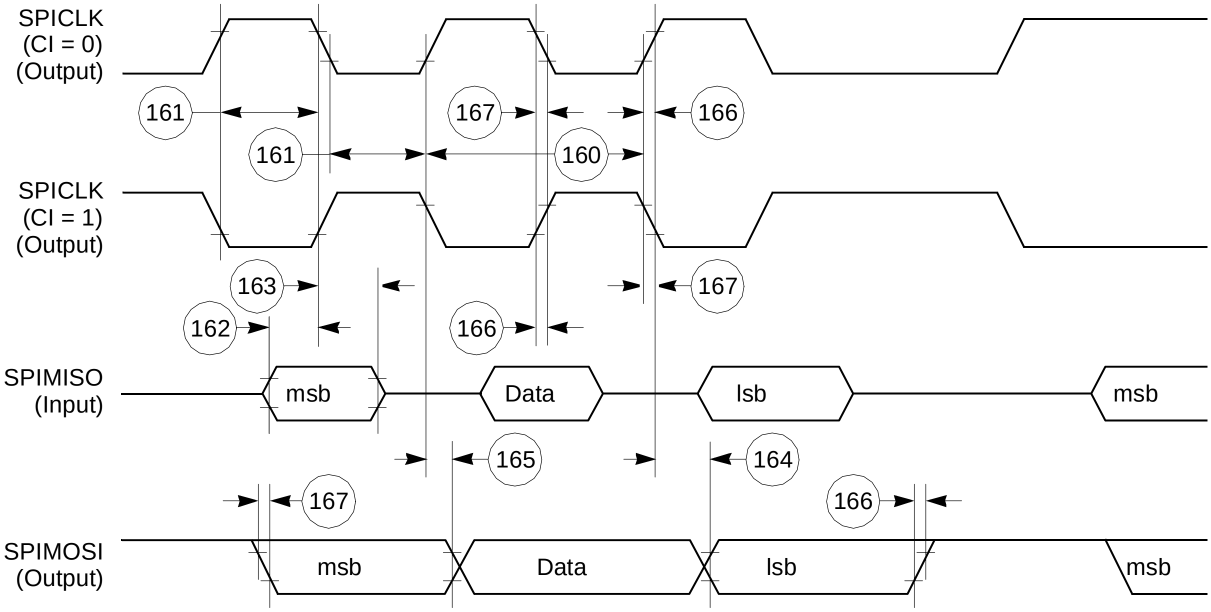


Figure 61. SPI Master (CP = 1) Timing Diagram

## 13.10 SPI Slave AC Electrical Specifications

Table 27 provides the SPI slave timings as shown in Figure 62 and Figure 63.

**Table 27. SPI Slave Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 170 | Slave cycle time | 2 | — | $t_{cyc}$ |
| 171 | Slave enable lead time | 15 | — | ns |
| 172 | Slave enable lag time | 15 | — | ns |
| 173 | Slave clock (SPICLK) high or low time | 1 | — | $t_{cyc}$ |
| 174 | Slave sequential transfer delay (does not require deselect) | 1 | — | $t_{cyc}$ |
| 175 | Slave data setup time (inputs) | 20 | — | ns |
| 176 | Slave data hold time (inputs) | 20 | — | ns |
| 177 | Slave access time | — | 50 | ns |

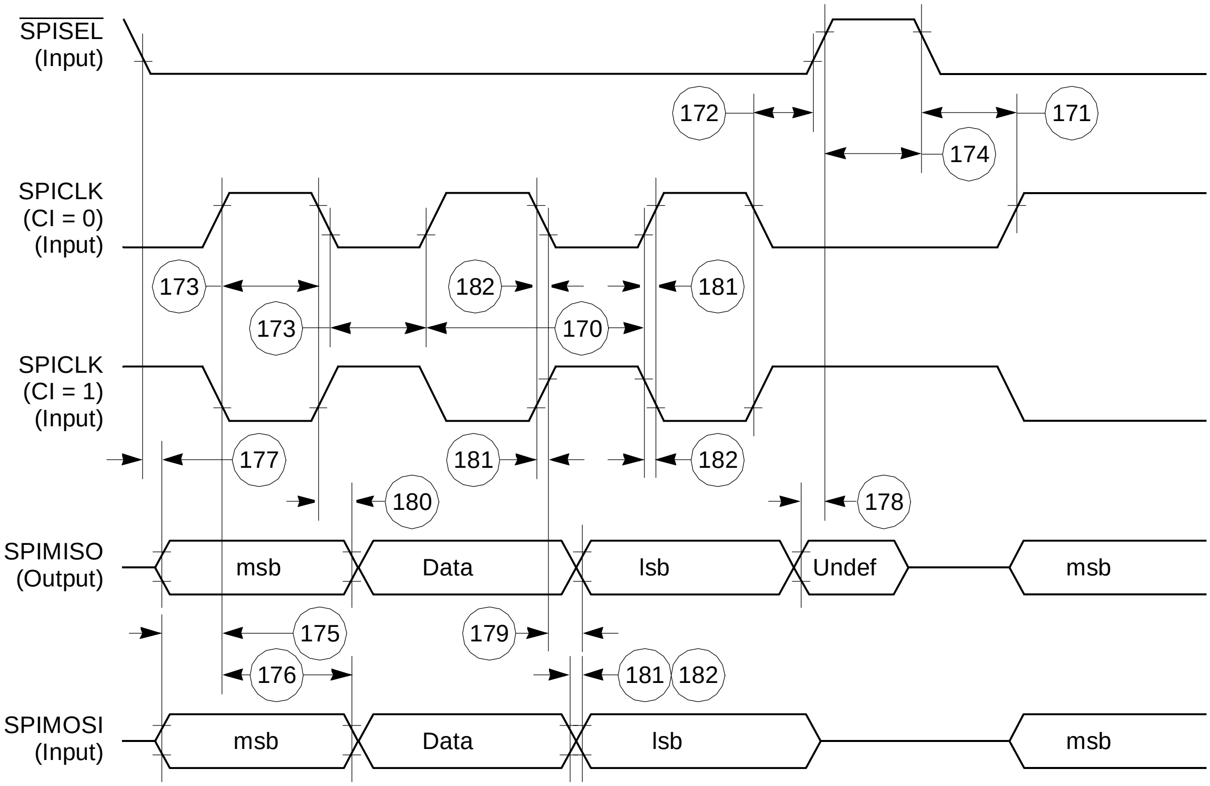


Figure 62. SPI Slave (CP = 0) Timing Diagram

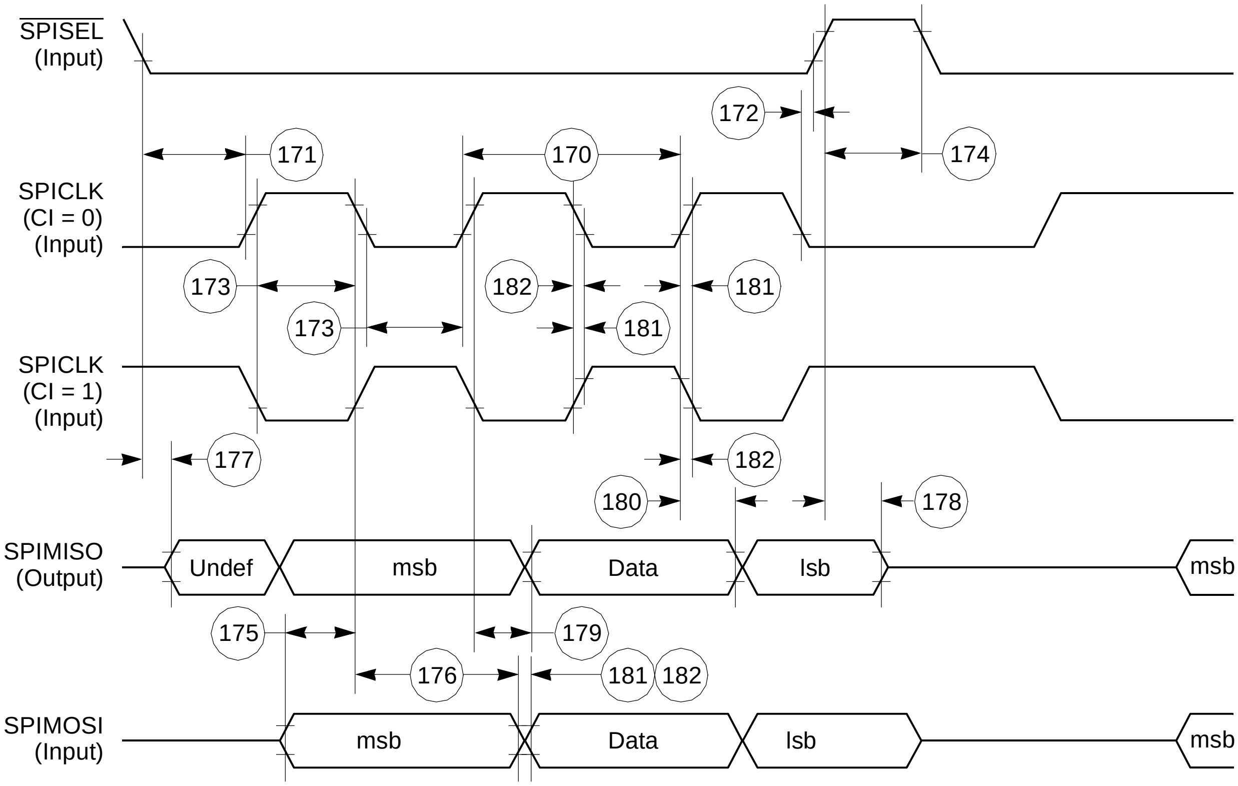


Figure 63. SPI Slave (CP = 1) Timing Diagram

## 13.11 I$^2$C AC Electrical Specifications

Table 28 provides the I$^2$C (SCL < 100 kHz) timings.

Table 28. I$^2$C Timing (SCL < 100 kHz)

| Num | Characteristic | All Frequencies |  | Unit |
|---|---|---|---|---|
|  |  | Min | Max |  |
| 200 | SCL clock frequency (slave) | 0 | 100 | kHz |
| 200 | SCL clock frequency (master)[1] | 1.5 | 100 | kHz |
| 202 | Bus free time between transmissions | 4.7 | — | µs |
| 203 | Low period of SCL | 4.7 | — | µs |
| 204 | High period of SCL | 4.0 | — | µs |
| 205 | Start condition setup time | 4.7 | — | µs |
| 206 | Start condition hold time | 4.0 | — | µs |
| 207 | Data hold time | 0 | — | µs |
| 208 | Data setup time | 250 | — | ns |
| 209 | SDL/SCL rise time | — | 1 | µs |

**Table 28. I$^{2}$C Timing (SCL < 100 kHz) (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 210 | SDL/SCL fall time | — | 300 | ns |
| 211 | Stop condition setup time | 4.7 | — | µs |

[1] SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Table 29 provides the I$^{2}$C (SCL > 100 kHz) timings.

**Table 29. I$^{2}$C Timing (SCL > 100 kHz)**

| Num | Characteristic | Expression | All Frequencies | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master)[1] | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | — | 1/(2.2 × fSCL) | — | s |
| 203 | Low period of SCL | — | 1/(2.2 × fSCL) | — | s |
| 204 | High period of SCL | — | 1/(2.2 × fSCL) | — | s |
| 205 | Start condition setup time | — | 1/(2.2 × fSCL) | — | s |
| 206 | Start condition hold time | — | 1/(2.2 × fSCL) | — | s |
| 207 | Data hold time | — | 0 | — | s |
| 208 | Data setup time | — | 1/(40 × fSCL) | — | s |
| 209 | SDL/SCL rise time | — | — | 1/(10 × fSCL) | s |
| 210 | SDL/SCL fall time | — | — | 1/(33 × fSCL) | s |
| 211 | Stop condition setup time | — | 1/2(2.2 × fSCL) | — | s |

[1] SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scalar × 2).
The ratio SYNCCLK/(BRGCLK/pre_scalar) must be greater than or equal to 4/1.

Figure 64 shows the I$^{2}$C bus timing.

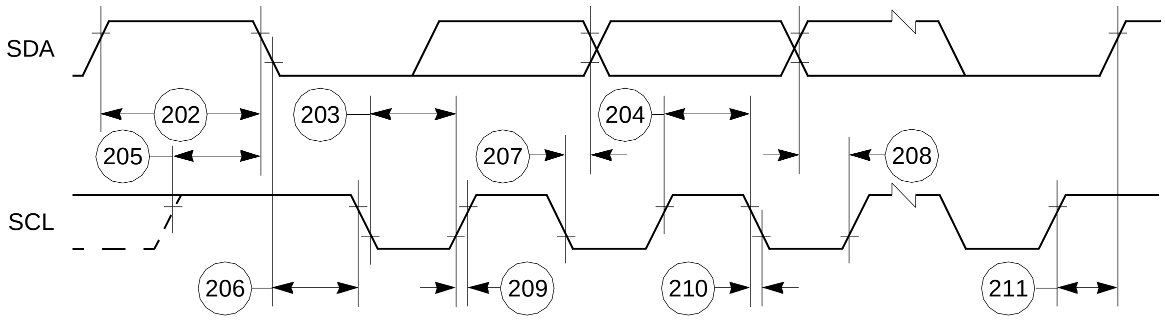


Figure 64. I$^{2}$C Bus Timing Diagram

# 14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

## 14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 30 lists the USB interface timings.

**Table 30. USB Interface AC Timing Specifications**

| Name | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| US1 | USBCLK frequency of operation[1]<br>Low speed<br>Full speed | <br>6<br>48 | | MHz |
| US4 | USBCLK duty cycle (measured at 1.5 V) | 45 | 55 | % |

[1] USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

# 15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

## 15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 31 provides information on the MII receive signal timing.

**Table 31. MII Receive Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M1 | MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup | 5 | — | ns |
| M2 | MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold | 5 | — | ns |
| M3 | MII_RX_CLK pulse width high | 35% | 65% | MII_RX_CLK period |
| M4 | MII_RX_CLK pulse width low | 35% | 65% | MII_RX_CLK period |
| M1_RMII | RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup | 4 | — | ns |
| M2_RMII | RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold | 2 | — | ns |

Figure 65 shows MII receive signal timing.

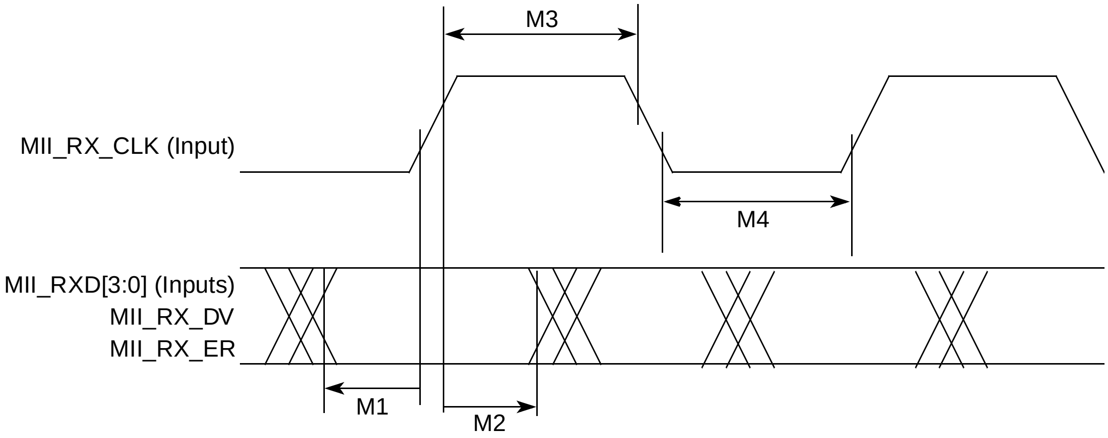


**Figure 65. MII Receive Signal Timing Diagram**

## 15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 32 provides information on the MII transmit signal timing.

**Table 32. MII Transmit Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M5 | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid | 5 | — | ns |
| M6 | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid | — | 25 | ns |
| M7 | MII_TX_CLK pulse width high | 35% | 65% | MII_TX_CLK period |
| M8 | MII_TX_CLK pulse width low | 35% | 65% | MII_TX_CLK period |
| M20_RMII | RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup | 4 | — | ns |
| M21_RMII | RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge | 2 | — | ns |

Figure 66 shows the MII transmit signal timing diagram.

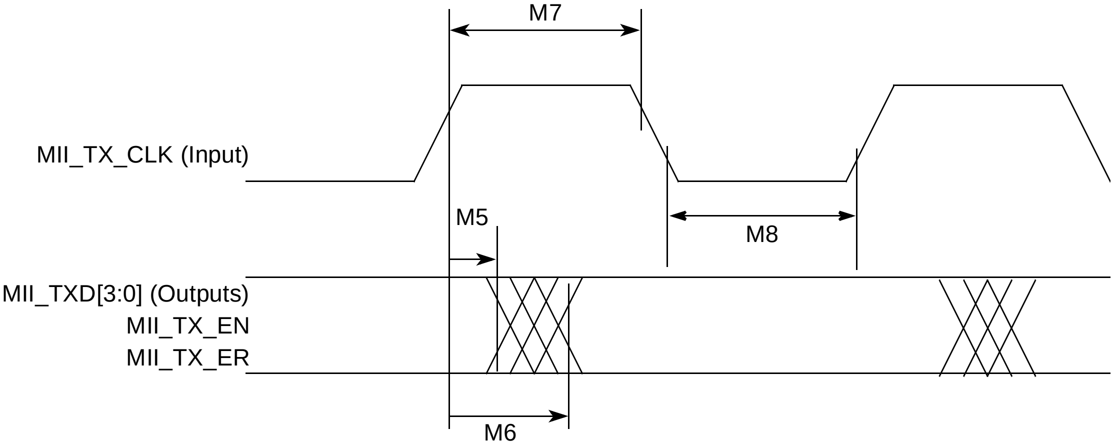


**Figure 66. MII Transmit Signal Timing Diagram**

## 15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 33 provides information on the MII async inputs signal timing.

**Table 33. MII Async Inputs Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M9 | MII_CRS, MII_COL minimum pulse width | 1.5 | — | MII_TX_CLK period |

Figure 67 shows the MII asynchronous inputs signal timing diagram.

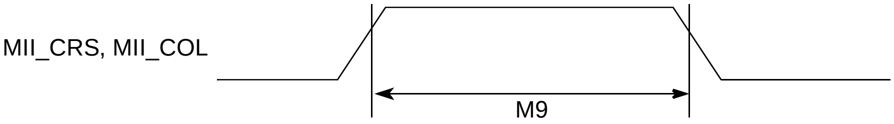


**Figure 67. MII Async Inputs Timing Diagram**

## 15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 34 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

**Table 34. MII Serial Management Channel Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M10 | MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | MII_MDC falling edge to MII_MDIO output valid (max prop delay) | — | 25 | ns |
| M12 | MII_MDIO (input) to MII_MDC rising edge setup | 10 | — | ns |
| M13 | MII_MDIO (input) to MII_MDC rising edge hold | 0 | — | ns |
| M14 | MII_MDC pulse width high | 40% | 60% | MII_MDC period |
| M15 | MII_MDC pulse width low | 40% | 60% | MII_MDC period |

Figure 68 shows the MII serial management channel timing diagram.

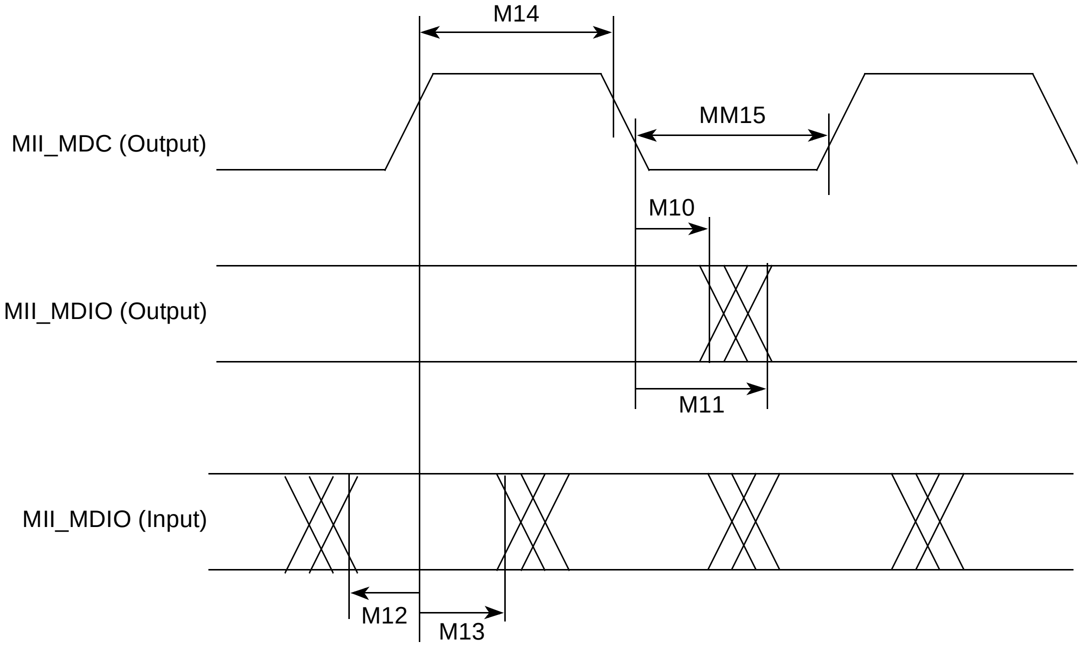


**Figure 68. MII Serial Management Channel Timing Diagram**

# 16 Mechanical Data and Ordering Information

Table 35 identifies the packages and operating frequencies available for the MPC875/MPC870.

**Table 35. Available MPC875/MPC870 Packages/Frequencies**

| Package Type | Temperature ($T_J$) | Frequency (MHz) | Order Number |
|---|---|---|---|
| Plastic ball grid array<br>ZT suffix—Leaded<br>VR suffix—Lead-Free are available as needed | 0°C to 95°C | 66 | KMPC875ZT66<br>KMPC870ZT66<br>MPC875ZT66<br>MPC870ZT66 |
| | | 80 | KMPC875ZT80<br>KMPC870ZT80<br>MPC875ZT80<br>MPC870ZT80 |
| | | 133 | KMPC875ZT133<br>KMPC870ZT133<br>MPC875ZT133<br>MPC870ZT133 |
| Plastic ball grid array<br>CZT suffix—Leaded<br>CVR suffix—Lead-Free are available as needed | -40°C to 100°C | 66 | KMPC875CZT66<br>KMPC870CZT66<br>MPC875CZT66<br>MPC870CZT66 |
| | | 133 | KMPC875CZT133<br>KMPC870CZT133<br>MPC875CZT133<br>MPC870CZT133 |

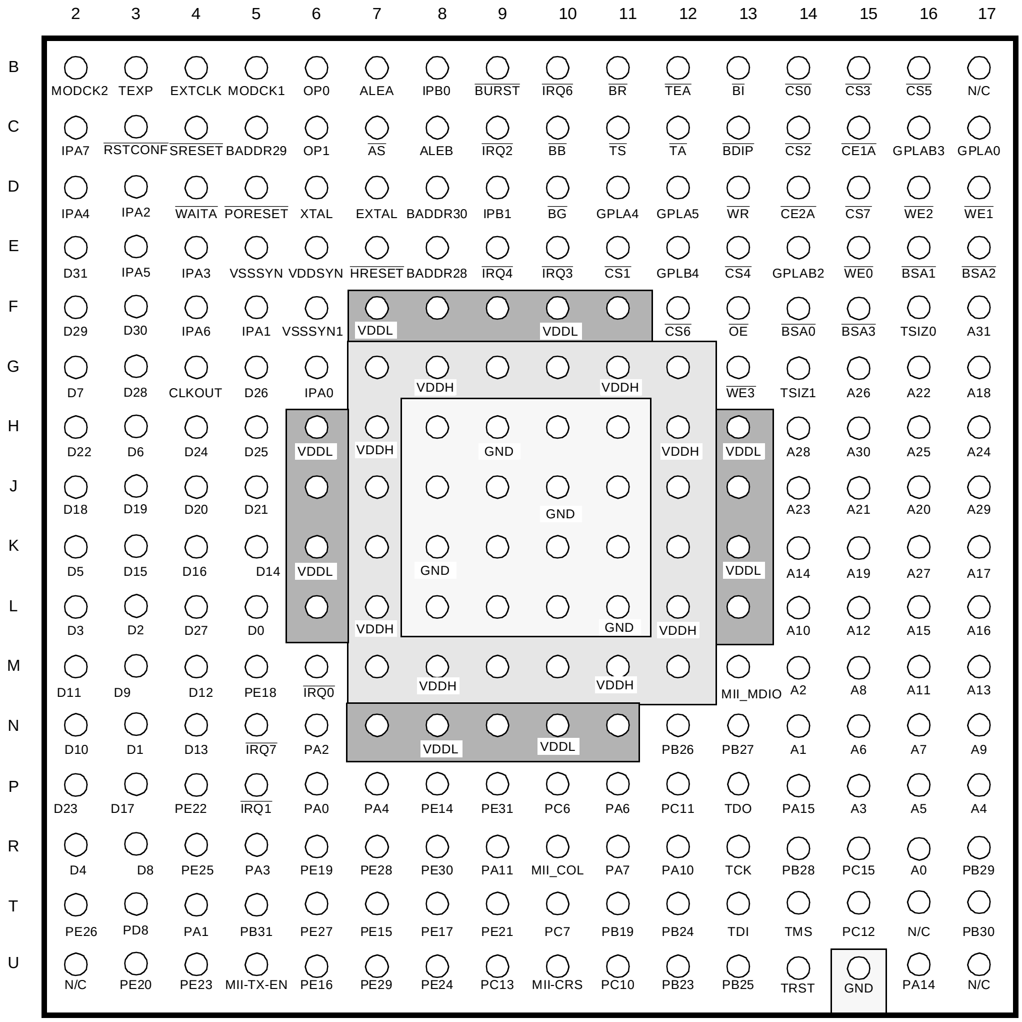
## 16.1 Pin Assignments

Figure 69 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC885 PowerQUICC Family User's Manual*.

**NOTE**

The pin numbering starts with B2 in order to conform to the JEDEC standard for 23-mm body size using a 16 × 16 array.

**NOTE:** This is the top view of the device.



| | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B | MODCK2 | TEXP | EXTCLK | MODCK1 | OP0 | ALEA | IPB0 | BURST | IRQ6 | BR | TEA | BI | CS0 | CS3 | CS5 | N/C |
| C | IPA7 | RSTCONF | SRESET | BADDR29 | OP1 | AS | ALEB | IRQ2 | BB | TS | TA | BDIP | CS2 | CE1A | GPLAB3 | GPLA0 |
| D | IPA4 | IPA2 | WAITA | PORESET | XTAL | EXTAL | BADDR30 | IPB1 | BG | GPLA4 | GPLA5 | WR | CE2A | CS7 | WE2 | WE1 |
| E | D31 | IPA5 | IPA3 | VSSSYN | VDDSYN | HRESET | BADDR28 | IRQ4 | IRQ3 | CS1 | GPLB4 | CS4 | GPLAB2 | WE0 | BSA1 | BSA2 |
| F | D29 | D30 | IPA6 | IPA1 | VSSSYN1 | VDDL | | | VDDL | | CS6 | OE | BSA0 | BSA3 | TSIZ0 | A31 |
| G | D7 | D28 | CLKOUT | D26 | IPA0 | | VDDH | | | VDDH | | WE3 | TSIZ1 | A26 | A22 | A18 |
| H | D22 | D6 | D24 | D25 | VDDL | VDDH | | GND | | | VDDH | VDDL | A28 | A30 | A25 | A24 |
| J | D18 | D19 | D20 | D21 | | | | | GND | | | | A23 | A21 | A20 | A29 |
| K | D5 | D15 | D16 | D14 | VDDL | | GND | | | | | VDDL | A14 | A19 | A27 | A17 |
| L | D3 | D2 | D27 | D0 | | VDDH | | | | GND | VDDH | | A10 | A12 | A15 | A16 |
| M | D11 | D9 | D12 | PE18 | IRQ0 | | VDDH | | | VDDH | | MII_MDIO | A2 | A8 | A11 | A13 |
| N | D10 | D1 | D13 | IRQ7 | PA2 | | VDDL | | VDDL | | PB26 | PB27 | A1 | A6 | A7 | A9 |
| P | D23 | D17 | PE22 | IRQ1 | PA0 | PA4 | PE14 | PE31 | PC6 | PA6 | PC11 | TDO | PA15 | A3 | A5 | A4 |
| R | D4 | D8 | PE25 | PA3 | PE19 | PE28 | PE30 | PA11 | MII_COL | PA7 | PA10 | TCK | PB28 | PC15 | A0 | PB29 |
| T | PE26 | PD8 | PA1 | PB31 | PE27 | PE15 | PE17 | PE21 | PC7 | PB19 | PB24 | TDI | TMS | PC12 | N/C | PB30 |
| U | N/C | PE20 | PE23 | MII-TX-EN | PE16 | PE29 | PE24 | PC13 | MII-CRS | PC10 | PB23 | PB25 | TRST | GND | PA14 | N/C |

Figure 69. Pinout of the PBGA Package—JEDEC Standard

Table 36 contains a list of the MPC875/MPC870 input and output signals and shows multiplexing and pin assignments.

**Table 36. Pin Assignments—JEDEC Standard**

| Name | Pin Number | Type |
|---|---|---|
| A[0:31] | R16, N14, M14, P15, P17, P16, N15, N16, M15, N17, L14, M16, L15, M17, K14, L16, L17, K17, G17, K15, J16, J15, G16, J14, H17, H16, G15, K16, H14, J17, H15, F17 | Bidirectional<br>Three-state (3.3 V only) |
| TSIZ0, REG | F16 | Bidirectional<br>Three-state (3.3 V only) |
| TSIZ1 | G14 | Bidirectional<br>Three-state (3.3 V only) |
| RD/WR | D13 | Bidirectional<br>Three-state (3.3 V only) |
| BURST | B9 | Bidirectional<br>Three-state (3.3 V only) |
| BDIP, GPL_B5 | C13 | Output |
| TS | C11 | Bidirectional<br>Active pull-up (3.3 V only) |
| TA | C12 | Bidirectional<br>Active pull-up (3.3 V only) |
| TEA | B12 | Open-drain |
| BI | B13 | Bidirectional<br>Active pull-up (3.3 V only) |
| IRQ2, RSV | C9 | Bidirectional<br>Three-state (3.3 V only) |
| IRQ4, KR, RETRY, SPKROUT | E9 | Bidirectional<br>Three-state (3.3 V only) |
| D[0:31] | L5, N3, L3, L2, R2, K2, H3, G2, R3, M3, N2, M2, M4, N4, K5, K3, K4, P3, J2, J3, J4, J5, H2, P2, H4, H5, G5, L4, G3, F2, F3, E2 | Bidirectional<br>Three-state (3.3 V only) |
| CR, IRQ3 | E10 | Input |
| FRZ, IRQ6 | B10 | Bidirectional<br>Three-state (3.3 V only) |
| BR | B11 | Bidirectional (3.3 V only) |
| BG | D10 | Bidirectional (3.3 V only) |
| BB | C10 | Bidirectional<br>Active pull-up (3.3 V only) |
| IRQ0 | M6 | Input (3.3 V only) |
| IRQ1 | P5 | Input (3.3 V only) |
| IRQ7 | N5 | Input (3.3 V only) |
| CS[0:5] | B14, E11, C14, B15, E13, B16 | Output |

### Table 36. Pin Assignments—JEDEC Standard (continued)

| Name | Pin Number | Type |
|---|---|---|
| CS6, CE1_B | F12 | Output |
| CS7, CE2_B | D15 | Output |
| WE0, BS_B0, IORD | E15 | Output |
| WE1, BS_B1, IOWR | D17 | Output |
| WE2, BS_B2, PCOE | D16 | Output |
| WE3, BS_B3, PCWE | G13 | Output |
| BS_A[0:3] | F14, E16, E17, F15 | Output |
| GPL_A0, GPL_B0 | C17 | Output |
| OE, GPL_A1, GPL_B1 | F13 | Output |
| GPL_A[2:3], GPL_B[2:3], CS[2–3] | E14, C16 | Output |
| UPWAITA, GPL_A4 | D11 | Bidirectional (3.3 V only) |
| UPWAITB, GPL_B4 | E12 | Bidirectional |
| GPL_A5 | D12 | Output |
| PORESET | D5 | Input (3.3 V only) |
| RSTCONF | C3 | Input (3.3 V only) |
| HRESET | E7 | Open-drain |
| SRESET | C4 | Open-drain |
| XTAL | D6 | Analog output |
| EXTAL | D7 | Analog input (3.3 V only) |
| CLKOUT | G4 | Output |
| EXTCLK | B4 | Input (3.3 V only) |
| TEXP | B3 | Output |
| ALE_A | B7 | Output |
| CE1_A | C15 | Output |
| CE2_A | D14 | Output |
| WAIT_A | D4 | Input (3.3 V only) |
| IP_A0 | G6 | Input (3.3 V only) |
| IP_A1 | F5 | Input (3.3 V only) |
| IP_A2, IOIS16_A | D3 | Input (3.3 V only) |
| IP_A3 | E4 | Input (3.3 V only) |
| IP_A4 | D2 | Input (3.3 V only) |
| IP_A5 | E3 | Input (3.3 V only) |

### Table 36. Pin Assignments—JEDEC Standard (continued)

| Name | Pin Number | Type |
|---|---|---|
| IP_A6 | F4 | Input (3.3 V only) |
| IP_A7 | C2 | Input (3.3 V only) |
| ALE_B, DSCK | C8 | Bidirectional<br>Three-state (3.3 V only) |
| IP_B[0:1], IWP[0:1], VFLS[0:1] | B8, D9 | Bidirectional (3.3 V only) |
| OP0 | B6 | Bidirectional (3.3 V only) |
| OP1 | C6 | Output |
| OP2, MODCK1, $\overline{\text{STS}}$ | B5 | Bidirectional (3.3 V only) |
| OP3, MODCK2, DSDO | B2 | Bidirectional (3.3 V only) |
| BADDR[28:29] | E8, C5 | Output |
| BADDR30, $\overline{\text{REG}}$ | D8 | Output |
| $\overline{\text{AS}}$ | C7 | Input (3.3 V only) |
| PA15, USBRXD | P14 | Bidirectional |
| PA14, USBOE | U16 | Bidirectional<br>(Optional: open-drain) |
| PA11, RXD4, MII1-TXD0, RMII1-TXD0 | R9 | Bidirectional<br>(Optional: open-drain)<br>(5-V tolerant) |
| PA10, MII1-TXERR, TIN4, CLK7 | R12 | Bidirectional<br>(Optional: open-drain)<br>(5-V tolerant) |
| PA7, CLK1, BRGO1, TIN1 | R11 | Bidirectional |
| PA6, CLK2, $\overline{\text{TOUT1}}$ | P11 | Bidirectional |
| PA4, $\overline{\text{CTS4}}$, MII1-TXD1, RMII-TXD1 | P7 | Bidirectional |
| PA3, MII1-RXER, RMII1-RXER, BRGO3 | R5 | Bidirectional<br>(5-V tolerant) |
| PA2, MII1-RXDV, RMII1-CRS_DV, TXD4 | N6 | Bidirectional<br>(5-V tolerant) |
| PA1, MII1-RXD0, RMII1-RXD0, BRGO4 | T4 | Bidirectional<br>(5-V tolerant) |
| PA0, MII1-RXD1, RMII1-RXD1, TOUT4 | P6 | Bidirectional<br>(5-V tolerant) |
| PB31, $\overline{\text{SPISEL}}$, MII1-TXCLK, RMII1-REFCLK | T5 | Bidirectional<br>(Optional: open-drain)<br>(5-V tolerant) |

### Table 36. Pin Assignments—JEDEC Standard (continued)

| Name | Pin Number | Type |
|---|---|---|
| PB30, SPICLK | T17 | Bidirectional<br>(Optional: open-drain)<br>(5-V tolerant) |
| PB29, SPIMOSI | R17 | Bidirectional<br>(Optional: open-drain)<br>(5-V tolerant) |
| PB28, SPIMISO, BRGO4 | R14 | Bidirectional<br>(Optional: open-drain)<br>(5-V tolerant) |
| PB27, I2CSDA, BRGO1 | N13 | Bidirectional<br>(Optional: open-drain) |
| PB26, I2CSCL, BRGO2 | N12 | Bidirectional<br>(Optional: open-drain) |
| PB25, SMTXD1 | U13 | Bidirectional<br>(Optional: open-drain)<br>(5-V tolerant) |
| PB24, SMRXD1 | T12 | Bidirectional<br>(Optional: open-drain)<br>(5-V tolerant) |
| PB23, $\overline{\text{SDACK1}}$, $\overline{\text{SMSYN1}}$ | U12 | Bidirectional<br>(Optional: open-drain) |
| PB19, MII1-RXD3, RTS4 | T11 | Bidirectional<br>(Optional: open-drain) |
| PC15, $\overline{\text{DREQ0}}$, L1ST1 | R15 | Bidirectional<br>(5-V tolerant) |
| PC13, MII1-TXD3, SDACK1 | U9 | Bidirectional<br>(5-V tolerant) |
| PC12, MII1-TXD2, TOUT1 | T15 | Bidirectional<br>(5-V tolerant) |
| PC11, USBRXP | P12 | Bidirectional |
| PC10, USBRXN, $\overline{\text{TGATE1}}$ | U11 | Bidirectional |
| PC7, $\overline{\text{CTS4}}$, L1TSYNCB, USBTXP | T10 | Bidirectional<br>(5-V tolerant) |
| PC6, $\overline{\text{CD4}}$, L1RSYNCB, USBTXN | P10 | Bidirectional<br>(5-V tolerant) |
| PD8, RXD4, MII-MDC, RMII-MDC | T3 | Bidirectional<br>(5-V tolerant) |
| PE31, CLK8, L1TCLKB, MII1-RXCLK | P9 | Bidirectional<br>(Optional: open-drain) |
| PE30, L1RXDB, MII1-RXD2 | R8 | Bidirectional<br>(Optional: open-drain) |

**Table 36. Pin Assignments—JEDEC Standard (continued)**

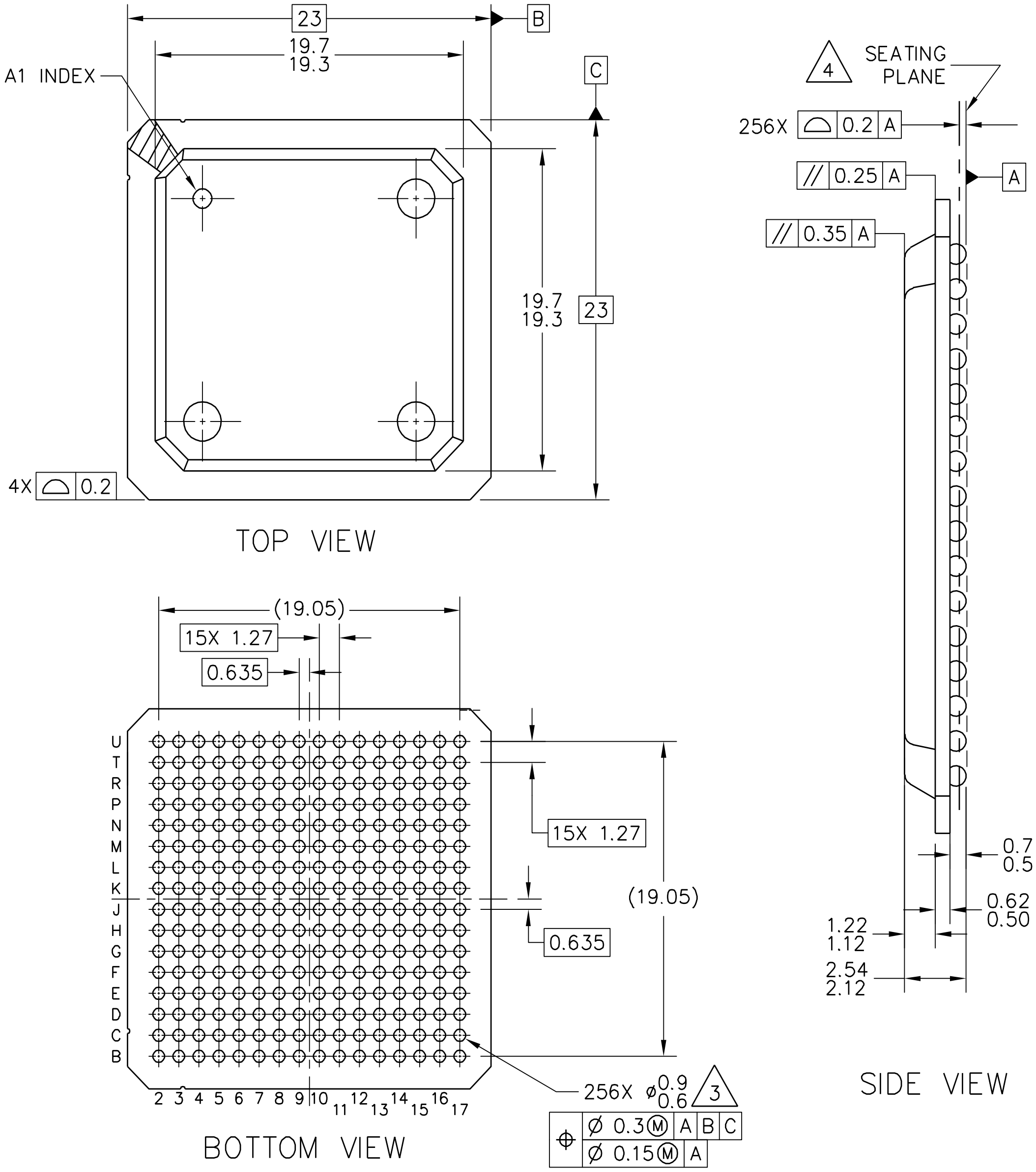
| Name | Pin Number | Type |
|---|---|---|
| PE29, MII2-CRS | U7 | Bidirectional<br>(Optional: open-drain) |
| PE28, $\overline{\text{TOUT3}}$, MII2-COL | R7 | Bidirectional<br>(Optional: open-drain) |
| PE27, L1RQB, MII2-RXERR, RMII2-RXERR | T6 | Bidirectional<br>(Optional: open-drain) |
| PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV | T2 | Bidirectional<br>(Optional: open-drain) |
| PE25, RXD4, MII2-RXD3, L1ST2 | R4 | Bidirectional<br>(Optional: open-drain) |
| PE24, SMRXD1, BRGO1, MII2-RXD2 | U8 | Bidirectional<br>(Optional: open-drain) |
| PE23, TXD4, MII2-RXCLK, L1ST1 | U4 | Bidirectional<br>(Optional: open-drain) |
| PE22, TOUT2, MII2-RXD1, RMII2-RXD1, SDACK1 | P4 | Bidirectional<br>(Optional: open-drain) |
| PE21, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0 | T9 | Bidirectional<br>(Optional: open-drain) |
| PE20, MII2-TXER | U3 | Bidirectional<br>(Optional: open-drain) |
| PE19, L1TXDB, MII2-TXEN, RMII2-TXEN | R6 | Bidirectional<br>(Optional: open-drain) |
| PE18, SMTXD1, MII2-TXD3 | M5 | Bidirectional<br>(Optional: open-drain) |
| PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2 | T8 | Bidirectional<br>(Optional: open-drain) |
| PE16, L1RCLKB, CLK6, MII2-TXCLK, RMII2-REFCLK | U6 | Bidirectional<br>(Optional: open-drain) |
| PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1 | T7 | Bidirectional |
| PE14, MII2-TXD0, RMII2-TXD0 | P8 | Bidirectional |
| TMS | T14 | Input<br>(5-V tolerant) |
| TDI, DSDI | T13 | Input<br>(5-V tolerant) |
| TCK, DSCK | R13 | Input<br>(5-V tolerant) |
| $\overline{\text{TRST}}$ | U14 | Input<br>(5-V tolerant) |

Table 36. Pin Assignments—JEDEC Standard (continued)

| Name | Pin Number | Type |
|---|---|---|
| TDO, DSDO | P13 | Output<br>(5-V tolerant) |
| MII1_CRS | U10 | Input |
| MII_MDIO | M13 | Bidirectional<br>(5-V tolerant) |
| MII1_TX_EN, RMII1_TX_EN | U5 | Output<br>(5-V tolerant) |
| MII1_COL | R10 | Input |
| $V_{SSSYN}$ | E5 | PLL analog GND |
| $V_{SSSYN1}$ | F6 | PLL analog GND |
| $V_{DDSYN}$ | E6 | PLL analog $V_{DD}$ |
| GND | H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, U15 | Power |
| $V_{DDL}$ | F7, F8, F9, F10, F11, H6, H13, J6, J13, K6, K13, L6, L13, N7, N8, N9, N10, N11 | Power |
| $V_{DDH}$ | G7, G8, G9, G10, G11, G12, H7, H12, J7, J12, K7, K12, L7, L12, M7, M8, M9, M10, M11, M12 | Power |
| N/C | B17, T16, U2, U17 | No connect |

## 16.2 Mechanical Dimensions of the PBGA Package

Figure 70 shows the mechanical dimensions of the PBGA package.



**NOTES:**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

**Note**: Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC875/MPC870VRXXX.
Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC875/MPC870ZTXXX.

**Figure 70. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package**

# 17 Document Revision History

Table 37 lists significant changes between revisions of this hardware specification.

**Table 37. Document Revision History**

| Revision Number | Date | Changes |
|---|---|---|
| 0 | 2/2003 | Initial release. |
| 0.1 | 3/2003 | Took out the time-slot assigner and changed the SCC for SCC3 to SCC4. |
| 0.2 | 5/2003 | Changed the package drawing, removed all references to Data Parity. Changed the SPI Master Timing Specs. 162 and 164. Added the RMII and USB timing. Added the 80-MHz timing. |
| 0.3 | 5/2003 | Made sure the pin types were correct. Changed the Features list to agree with the MPC885. |
| 0.4 | 5/2003 | Corrected the signals that had overlines on them. Made corrections on two pins that were typos. |
| 0.5 | 5/2003 | Changed the pin descriptions for PD8 and PD9. |
| 0.6 | 5/2003 | Changed a few typos. Put back the $I^2C$. Put in the new reset configuration, corrected the USB timing. |
| 0.7 | 6/2003 | Changed the pin descriptions per the June 22 spec, removed Utopia from the pin descriptions, changed PADIR, PBDIR, PCDIR and PDDIR to be 0 in the Mandatory Reset Config. |
| 0.8 | 8/2003 | Added the reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams. |
| 0.9 | 8/2003 | Changed the USB description to full-/low-speed compatible. |
| 1.0 | 9/2003 | Added the DSP information in the Features list.<br>Put a new sentence under Mechanical Dimensions.<br>Fixed table formatting.<br>Nontechnical edits.<br>Released to the external web. |
| 1.1 | 10/2003 | Added TDMb to the MPC875 Features list, the MPC875 Block Diagram, added 13.5 Serial Interface AC Electrical Specifications, and removed TDMa from the pin descriptions. |
| 2.0 | 12/2003 | Changed DBGC in the Mandatory Reset Configuration to X1.<br>Changed the maximum operating frequency to 133 MHz.<br>Put the timing in the 80 MHz column.<br>Put in the orderable part numbers.<br>Rounded the timings to hundredths in the 80 MHz column.<br>Put the pin numbers in footnotes by the maximum currents in Table 6.<br>Changed 22 and 41 in the Timing.<br>Put TBD in the Thermal table. |

Table 37. Document Revision History (continued)

| Revision Number | Date | Changes |
|---|---|---|
| 3.0 | 1/07/2004<br>7/19/2004 | • Added sentence to Spec B1A about EXTCLK and CLKOUT being in alignment for integer values.<br>• Added a footnote to Spec 41 specifying that EDM = 1.<br>• Added the thermal numbers to Table 4.<br>• Added RMII1_EN under M1II_EN in Table 36, Pin Assignments.<br>• Added a table footnote to Table 6, DC Electrical Specifications, about meeting the $V_{IL}$ Max of the $I^2C$ Standard.<br>• Put the new part numbers in the Ordering Information Section. |
| 4 | 08/2007 | • Updated template.<br>• On page 1, updated first paragraph and added a second paragraph.<br>• After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures.<br>• In Table 10, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz.<br>• In Figure 5, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level.<br>• In Table 18, changed num 46 description to read, “$\overline{\text{TA}}$ assertion to rising edge ...”<br>• In Figure 43, changed $\overline{\text{TA}}$ to reflect the rising edge of the clock. |

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Document Number: MPC875EC
Rev. 4
08/2007